A novel time register with process and temperature calibration

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***Abstract*—This paper presents a novel time register circuit suitable for time-based or time-domain signal processing. The proposed circuit is based on the capacitor discharging method and is compensated against technology process and chip temperature variations using a novel calibration loop based on master-slave approach. The loop contains a high-speed comparator based on simple current-starved inverter logic along with a triple-point threshold voltage stabilization loop. The circuit is designed using 28nm Samsung FD-SOI process under 1V supply voltage with 10MHz operating frequency. Simulation results present an almost constant capacitor voltage discharging slope of the time register over worst case process corners and temperature between 0ºC and 100ºC while consuming only 10μA.**

Keywords—Time-based, time-domain, time register, time delay calibration loops, CMOS, FD-SOI.

I. INTRODUCTION

Modern CMOS processes are mainly driven by digital intergraded circuits (IC) requirements for higher processing speed and lower power consumption featuring device sizes shrinking and low voltage supplies. Under these conditions analog design becomes more challenging due to smaller voltage headroom and due to this worse dynamic range. Time-domain circuit design is an advantageous approach of analog circuits for scaled technologies in terms of the trade-off between dynamic range and the power consumption, especially for high speed MOS devices, compared with the conventional voltage-domain or current-domain approach [1].

The time-based approach is a good candidate methodology for implementing power efficient circuit and system solutions mainly due to fact that the quantity of interest is the time and not the voltage or current as in all other approaches. Therefore, the signal processing achieved in time-domain instead of voltage and/or current domain [2].

The main benefits of this approach is the improved dynamic range and time resolution compared with the analog circuit under the same low supply environment [3], the power efficiency, the high-speed and low power performance because they are mainly composed of CMOS digital building blocks (gates etc.) [4].

Time-register (TR) is the main building block in the construction of time-based arithmetic circuits such as time amplifiers [5], time adders/subtractors, time-integrators and time-to-digital converters [6] unlike the prior state-of-the-art circuits which operate in phase domain [7], [8].

The basic goal of the time-register is capability to store time and recover it when needed. In order to achieve that, TR converts the information in time domain such as a pulse width or time difference between the pulse edges to a proportional voltage or current. State-of-the-art time registers are based a) on the single capacitor discharging through MOS devices [6] and b) on gated delay lines [9]. The first solution is more attractive compared to the inherent limitations of the gated delay lines since the circuit implementation is much simpler requiring fewer transistors, as well. The impact of leakage is the same between two solutions for high data rate cases [6].

The main problem of both solutions is the strong impact of the technology process (P) variations and chip temperature (T) corners (PT corners). The slope of the capacitor voltage discharging features strong variation over PT corners due to the fact that it is mainly dependent by the discharging drain current of a MOS device and by the on-chip capacitor. Any variation of the discharging slope will affect the accuracy of the time storing.

Our work proposes a modified capacitor discharging based time register which is more suitable for PT corners compensation along with a novel slope calibration loop over PT corners which is based on master-slave approach. The calibration loop includes also a novel high-speed comparator, a simple integrator based on differential pair and few digital gates. The high-speed comparator is based on tuned current-starved inverter with very stable triple-point threshold voltage taking advantage of master-slave approach again.

This paper is organized as follows. Operation principle and the implementation of the proposed time-register are described in Section II. Next, the high-speed comparator and its triple-point threshold voltage architecture are presented in Section III. Section IV reports the simulation results of the fast comparator and the entire time-register circuit performance.

II. NOVEL TIME REGISTER

A. Operation of novel time-register

The circuit of the time register which is based on the capacitor discharging concept is presented in Fig. 1(a) while the operating diagrams are presented in Fig. 1(b). The *SET* pulse pulls up the capacitor voltage to the supply voltage V_{DD}. The input information is described as an input pulse with width equal to T_{in}. Normally, a voltage-to-time converter is necessary to linearly convert an input voltage to a proportional pulse width T_{in}.

During the time interval of T_{in} the capacitor voltage is discharged. The time span of T_{CLK}, assuming that the slope stays the same, is constant. Therefore, the output of the circuit is T_{CLK}-T_{in} achieving in this manner the storing of the value of T_{in}.

The proposed time register is presented in Fig. 1(c). Transistor M_2 acts as a switch and transistor M_3 acts as current source. The advantage of the proposed structure is that the current of M_3 and hence the discharging slope can be easily defined through its gate voltage *CTRL*. As it will be explained later, the variation of the discharging slope can be compensated by adjusting accordingly voltage *CTRL* through a suitable negative feedback loop. If voltage *CTRL* decreases then the drain current decreases as well, and therefore, the discharging slope decreases. The last observation is used in order to calibrate the slope through adjusting voltage *CTRL*.

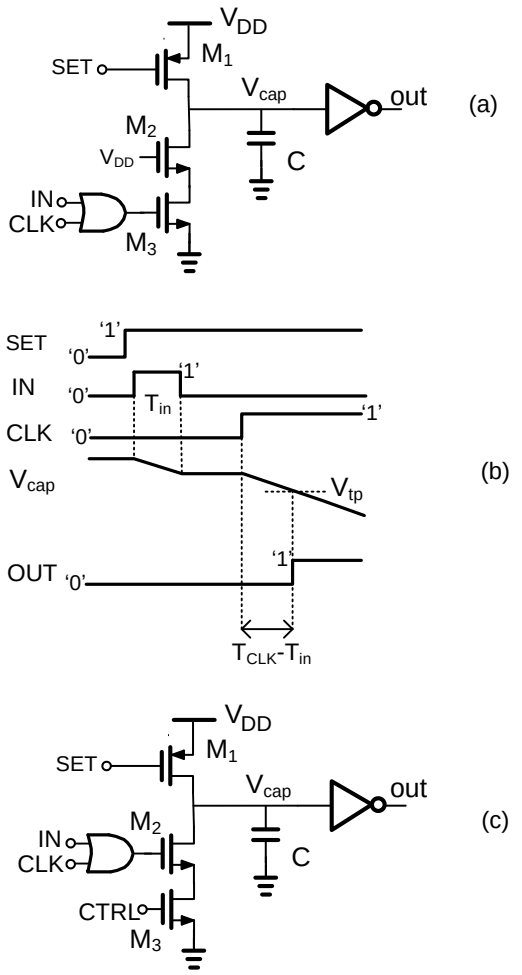

Fig. 1. a) Time register state-of-the-art circuit, b) operation, c) proposed time register

B. Implementation of the slope compensation loop

As discussed above the slope of the time register must be calibrated against PT corners in order to increase the accuracy of the time registration. The slope calibration architecture is intuitively presented in Fig.2. A replica of time register is used, which acts as Master Device. The discharging capacitor voltage V_{cap} is compared with a reference voltage V_R using a high-speed comparator. The D flip-flop is actually used as a phase-detector and compares the time delay between V_{comp} and *REF* negative pulse edges. *REF* clock signal applies the reference clock T_{ref} pulse width to the calibration loop. Their time difference is converted to current through transconductor g_m and integrated on the capacitor C_{CAL}. Voltage *CTRL* is built across capacitor C_{CAL}. The loop is locked when V_{comp} and *REF* negative pulse edges are synchronized which means that the average output current of transconductor is almost zero.

The basic waveforms which describe the operation principle of the calibration loop are presented in Fig. 3. In case (*i*), the discharging slope is small (in absolute value), V_{cap} not crosses V_R and V_{comp} never change voltage level (it stays at high logic state, '1'). In this case, the loop tends to increase voltage *CTRL* in order to increase the drain current of M_3 and, therefore, make the discharging slope sharpness. In case (*ii*), the discharging slope is too sharp, V_{cap} crosses V_R and V_{comp} change voltage level. In this case, the loop tends to decrease voltage *CTRL* in order to make slope less sharp. In both case (*i*) and (*ii*), the slope is away from the target slope but after a number of calibration steps the loop is locked. In case (*iii*), the slope reaches its final value which is indicated by the synchronization of V_{comp} and *REF* signals. In this case, the loop is locked, and voltage *CTRL* is settled to the final value.

Voltage *CTRL* is applied to the Slave time register after harmonics filtering using a simple low pass RC integrator a low pass filter (LPF). Therefore, both Master and Slave time register has identical discharging slope while the discharging slope will become stable over PT corners and equal to:

$$slope = \frac{V_{DD}-V_R}{T_{ref}} = \frac{I_{dis}}{C} \quad (1)$$

where I_{dis} is the discharging current which is defined by the channel geometry of M_3 and its gate voltage *CTRL*. It is obvious from eq.(1) that the slope can be easily adjusted accordingly with respect to the reference voltage V_R and the reference time period T_{ref}.

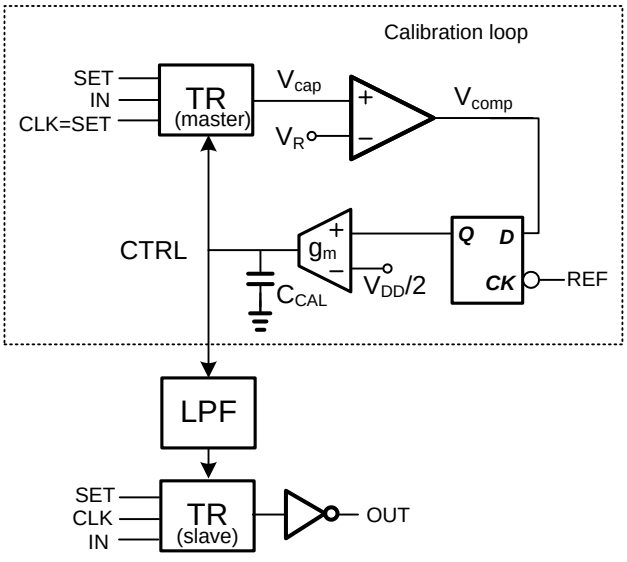

Fig. 2. System diagram of the master-slave slope calibration loop.

It should be mentioned that, in our implementation, Master and Slave is not necessary to be identical. The calibration loop can tune several Slave time registers at the

same time regarding the application. To save layout area, the discharging capacitor C in the Slave time register is N times smaller than that of the Master time register. Also, the channel width of M_2, M_3 at the Slave time register is N times smaller than those of the Master time register in order to give less discharging current. So, both Slave and Master time registers have the same discharging slope value but with less layout area needed for the Slave time register.

Also, the frequency which is used in the calibration loop is not necessary to be identical with the actual operation frequency of Slave time register. In this case, longer T_{ref} can be used but in addition to that larger discharging capacitor should also be used (only in the Slave time register). This way, eq.(1) is still valid while lower power dissipation for the calibration loop will be achieved making more efficient the proposed implementation.

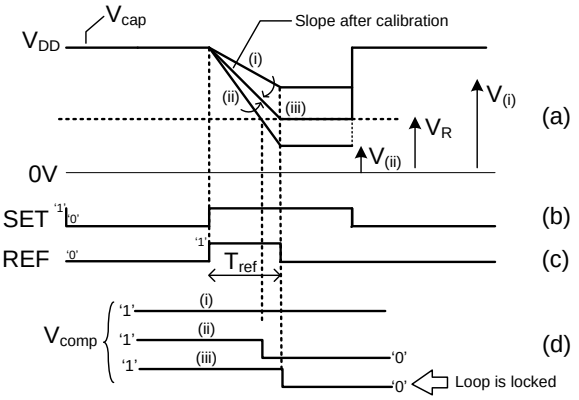

Fig. 3. Basic waveforms of the calibration loop, a) capacitor voltage, b) SET, c) REF and d) output of the comparator.

III. High Speed Comparator

The calibration loop needs a high speed and high accuracy comparator which it is also stable over the PT corners. A simple CMOS inverter is a good candidate to work as high-speed comparator, but its triple-point threshold voltage experiences large variation over PT corners. To tackle this problem a novel comparator based on the current starved inverter logic and utilizing the Master-slave technique was proposed.

The high-speed comparator is based on the current starved inverter as it is shown in Fig. 4(a). Since, the discharging slope of the time register must be calibrated across PT corners the comparator should be also stable across the same corners. The triple-point threshold voltage of a current-starved based inverter can be compensated by appropriate adjusting the gate voltage of the M_{n2}, M_{p2}. The compensation loop that is used to stabilize the triple point inverter is presented in Fig. 4(b).

As depicted in Fig. 4(b), the master circuit comprised by a starving current inverter and a single gain stage differential amplifier. The input of the inverter is biased at $V_{DD}/2$ while the stabilization loop will set the output at the same value over PT corners. As it shown in Fig. 4(b), the output of the inverter feeds an amplifier's input while at the other input the constant voltage $V_{DD}/2$ is applied. The amplifier's output which controls the gate of $M_{p2.ms}$, $M_{n2.ms}$ will make the proper adjustments in order to set the inverter's output at $V_{DD}/2$. The compensation loop stabilizes the triple point threshold voltage at around $V_{DD}/2$. It should be noted here that the frequency compensation network is not presented here for simplicity reasons.

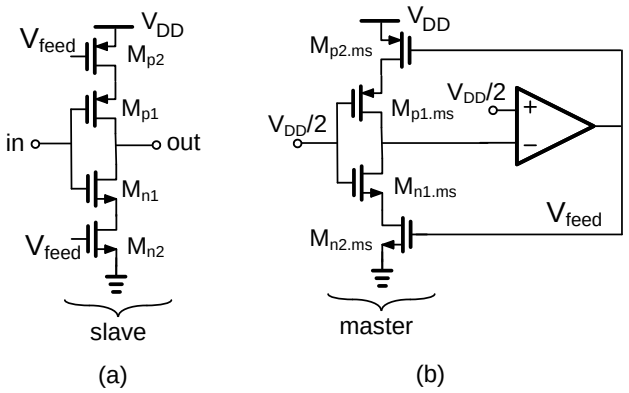

Fig. 4. a) High-speed current starver inverter and b) triple-point threshold voltage stabilization loop.

IV. Simulation Results

In order to verify the efficiency of the proposed circuit a time register, and a fast comparator have been designed and simulated in Samsung 28nm FD-SOI CMOS technology with a supply voltage 1V. The operation frequency of both Master TR and calibration loop was 10MHz. The N was equal to 2. The transient response of the calibration loop for time register is shown in Fig. 5. At the states (a) and (b) the slope is slower than needed so the loop continues to increase voltage *CTRL* until the slope has the correct value as depicted at the state (c). At this state the slope stays almost stable at the value of 10.056 MV/s. A ripple can be observed in Fig. 5, this happens because the locked loop oscillates between the closest values of the V_R.

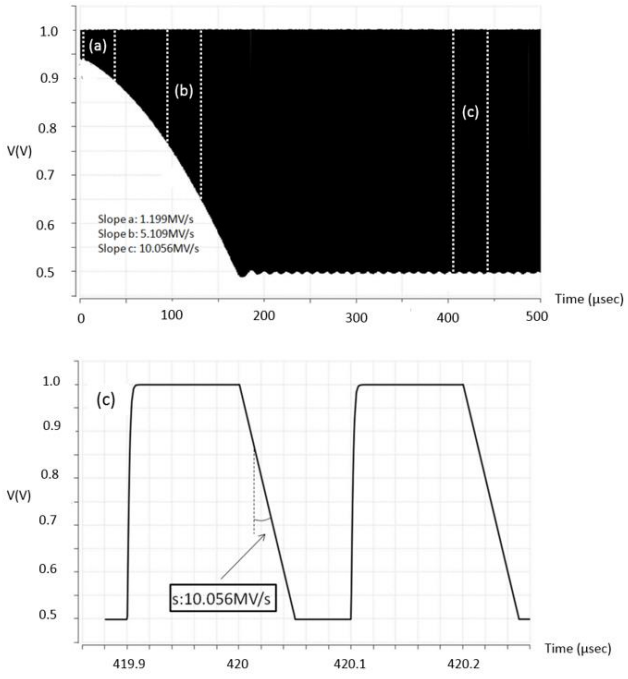

Fig. 5. Transient response of the calibration loop.

The whole purpose of the circuit is to keep the slope stable over PV corners. Slope values across process and temperature corners along comparison with the slope of regular time register are presented in TABLE I. The regular time register is presented in Fig. 1(a). The value of the slope is almost constant for the proposed time register with 0.48% variation contrary to the regular one which has 93.5% variation. Therefore, the proposed solution gives excellent slope stability and is expected to improve the linearity performance of time register over PT corners.

TABLE I. SLOPE STABILITY OVER PROCESS AND TEMPERATURE CORNERS

PV corner	Discharge slope(MV/s)	
	Proposed Time-register	***Regular Time-Register***
typ	10.056	10.010
Cmin_ff_0°	10.051	14.842
Cmin_ff_100°	10.066	12.192
Cmin_ss_0°	10.050	9.786
Cmin_ss_100°	10.044	8.071
Cmax_ff_0°	10.017	10.833
Cmax_ff_100°	10.035	8.448
Cmax_ss_0°	10.037	6.669
Cmax_ss_100°	10.059	5.478

Lastly, Fig. 6 presents the transient response across PT corners of the fast comparator by applying an input rump voltage. It is obvious that when the ramp crosses the value of 0.5V the inverter changes states from low to high. Thanks to calibration loop the triple-point threshold variation features very good stability over PT corners than that of the regular CMOS inverter. At the same time works a as very fast voltage comparator mainly due to its very simple structure.

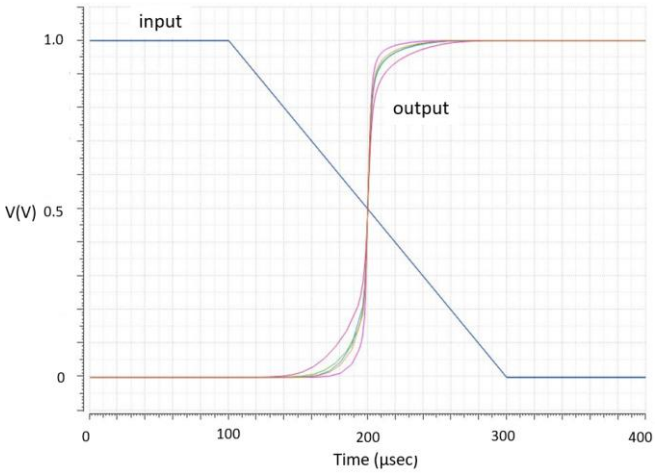

Fig. 6. Triple-point threshold voltage stabilization results over PT corners.

V. CONCLUSION

In this paper, a novel time register with process and temperature calibration is proposed. The proposed circuit uses the master-slave technique and achieves a constant discharge slope across PT corners presenting less than 0.48% variation. Comparison with regular time register gives major improvement. The circuit is designed to operate with 10MHz under 1V supply voltage. This time register opens the possibilities in designing time-based systems with process and temperature tolerance with it as the building block.

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