

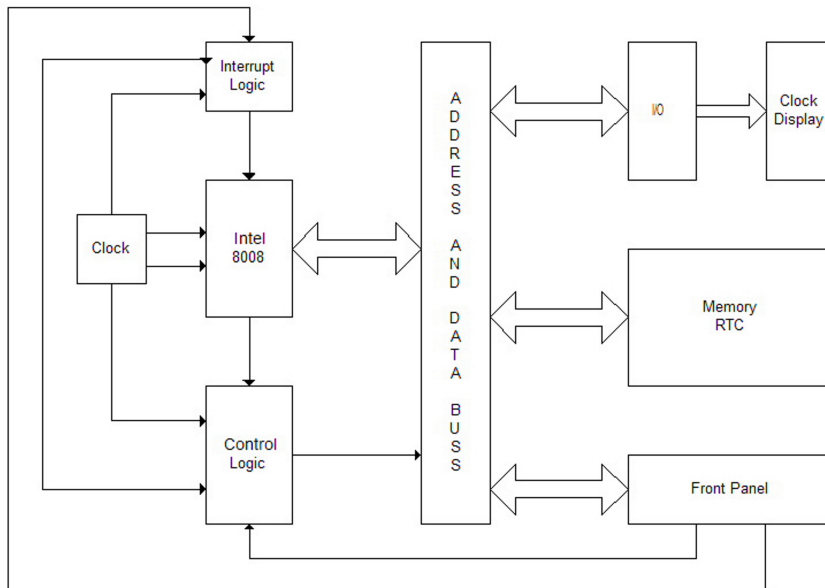
APXIZOME

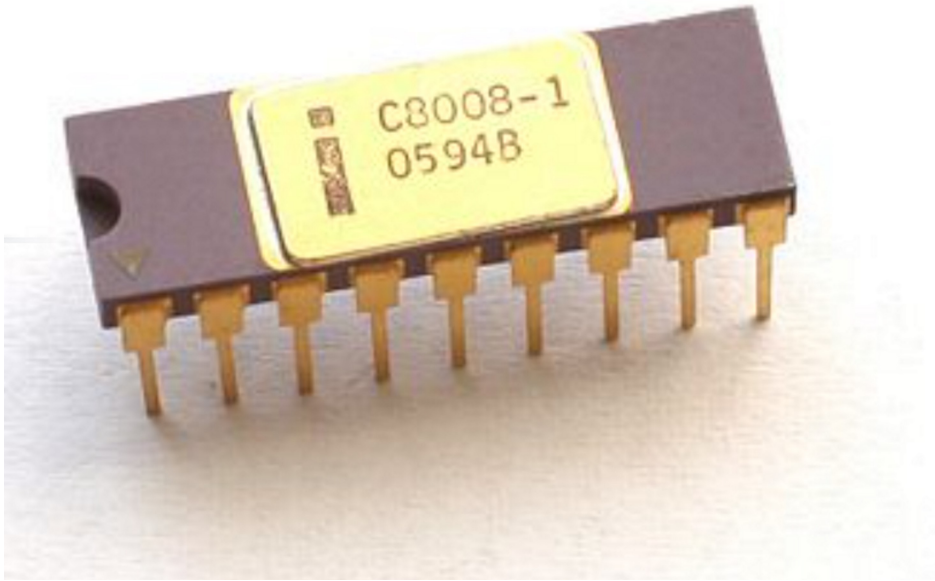
15:15

Address: 14 bits

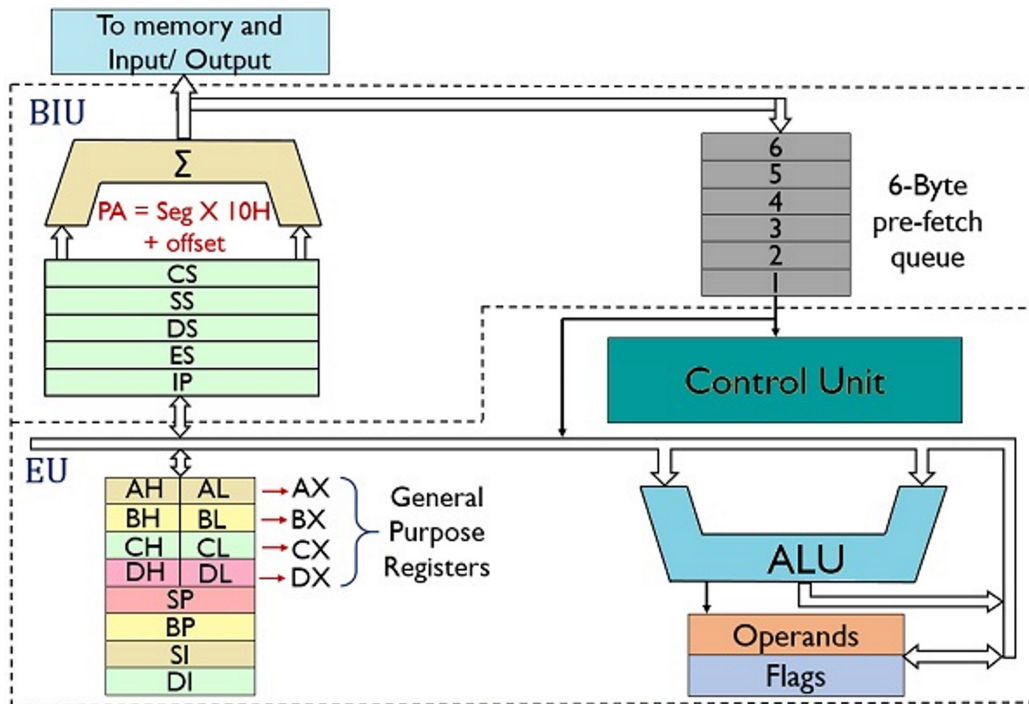
Data: 8 bits

Max. CPU clock rate 200 kHz to 800 kHz

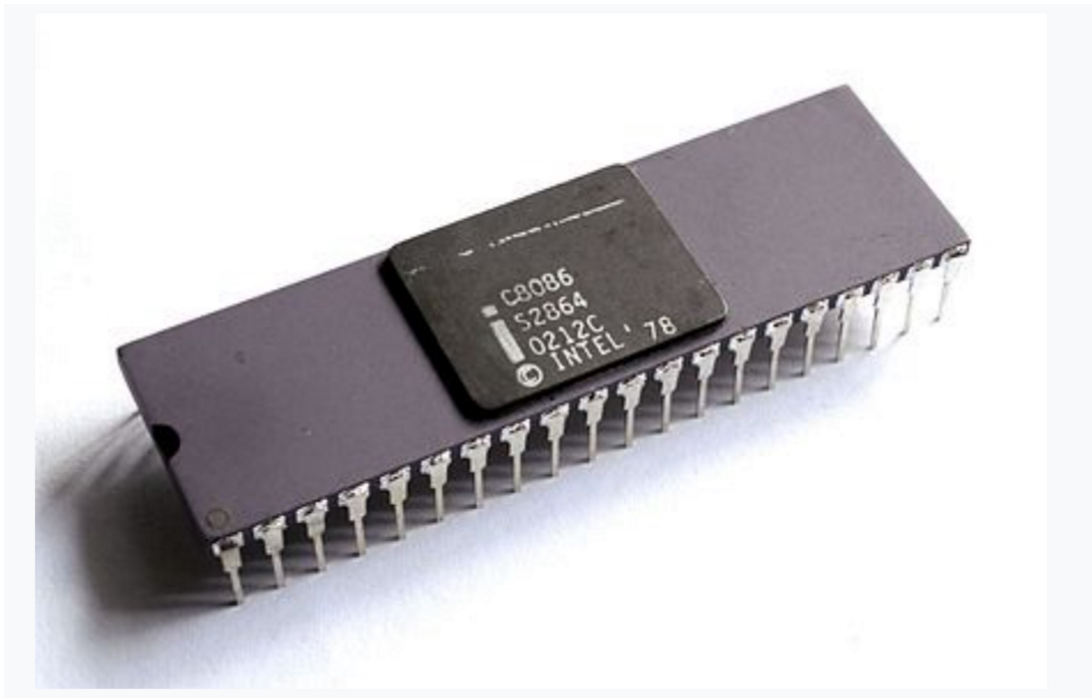




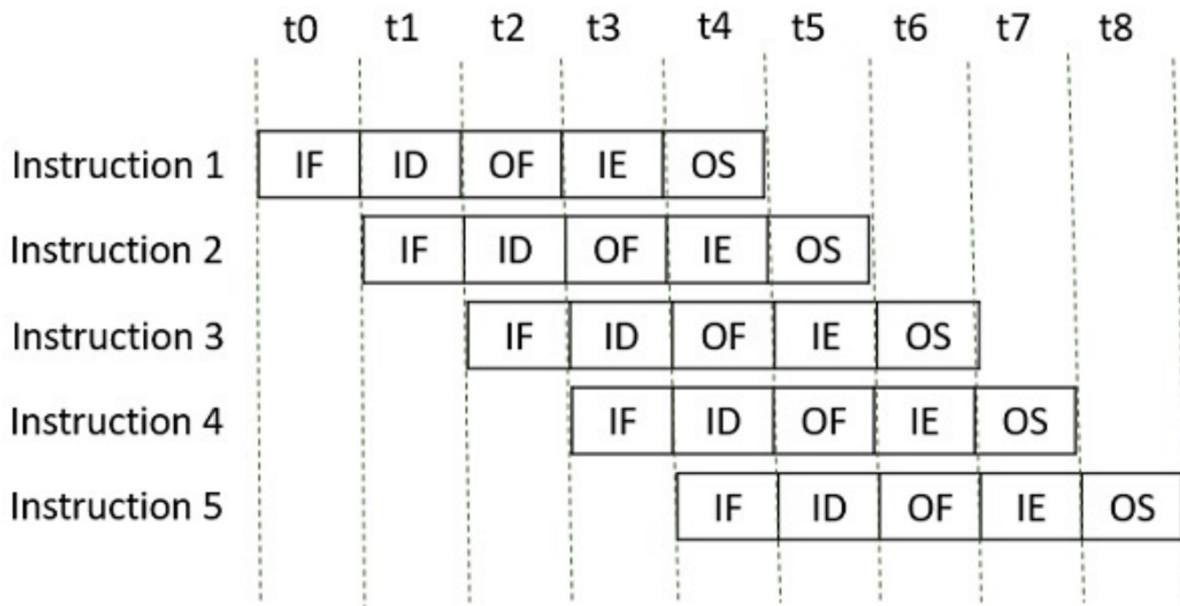
Address: 20 bits
 Data: 16 bits
 Max. CPU clock rate 5-10MHz
 Ο 8086 είχε 8 καταχωρητές γενικής χρήσης 16-bit



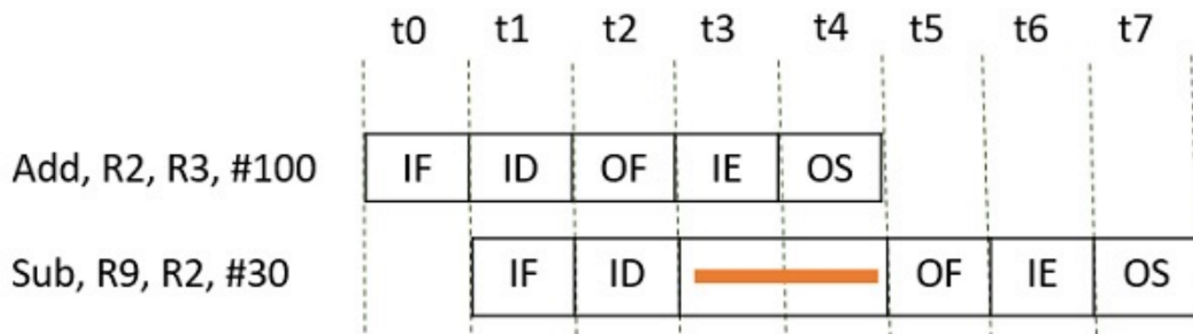
Block Diagram of 8086 Microprocessor



Instruction Fetch	Instruction Decode	Operand Fetch	Instruction Execute	Operand Store
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Pipelining of 5 Instructions

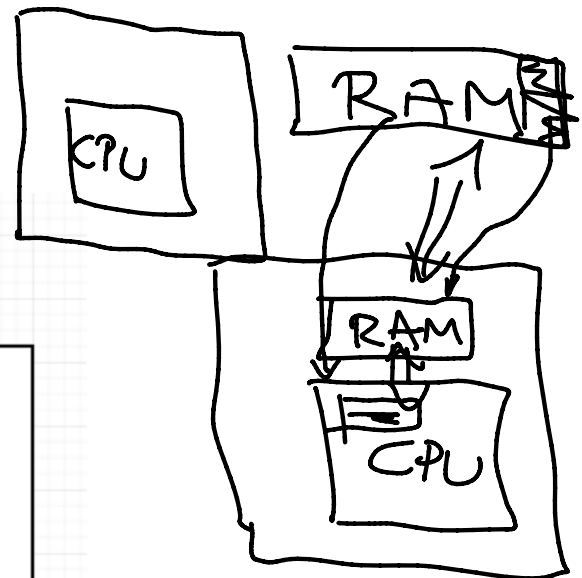


Data Dependency

CISC	RISC
It is prominent on Hardware	It is prominent on the Software
It has high cycles per second	It has low cycles per second
It has transistors used for storing Instructions which are complex	More transistors are used for storing memory
LOAD and STORE memory-to-memory is induced in instructions	LOAD and STORE register-register are independent
It has multi-clock	It has a single - clock

Flynn's taxonomy

		Instruction Streams	
		one	many
Data Streams	one	SISD traditional von Neumann single CPU computer	MISD May be pipelined Computers
	many	SIMD Vector processors fine grained data	MIMD Multi computers Multiprocessors



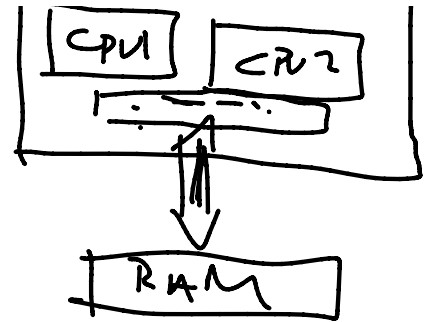
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Vector processors
fine grained data
Parallel computers

Multi computers
Multiprocessors

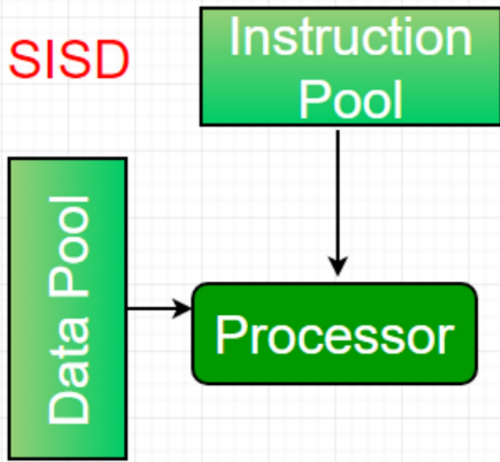
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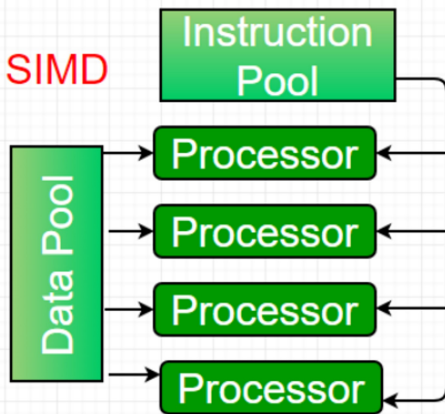


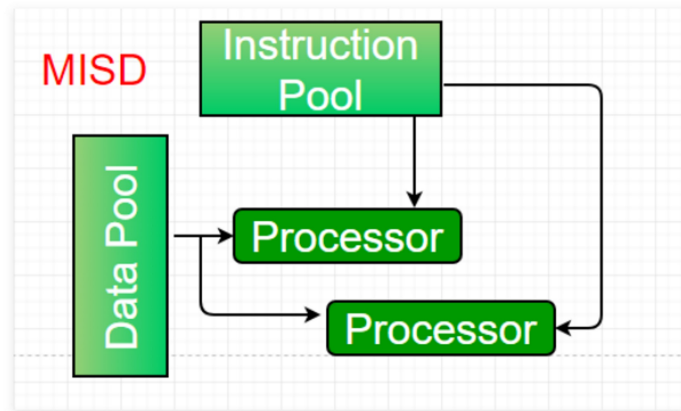
$$|x\rangle = \begin{matrix} \text{Sin}(y) \\ \uparrow \\ \text{CPU1} \end{matrix} + \begin{matrix} \text{Cos}(y) \\ \uparrow \\ \text{CPU2} \end{matrix}$$

SISD

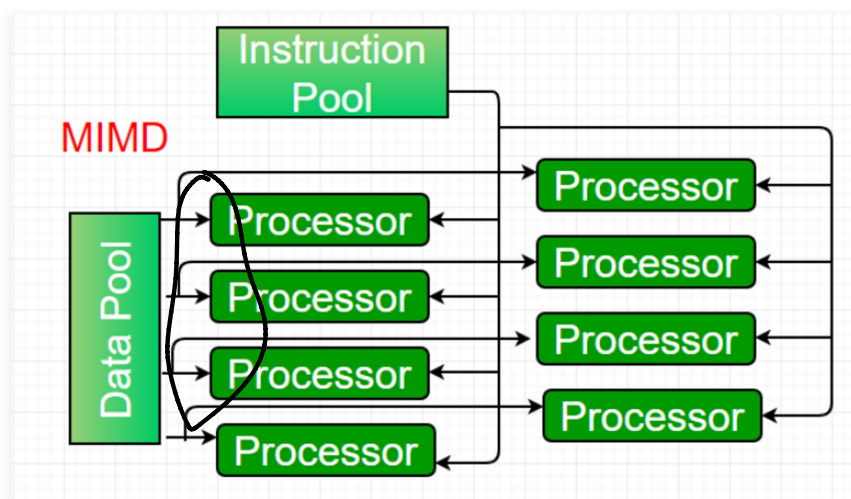


SIMD





Example $Z = \sin(x) + \cos(x) + \tan(x)$



MIMD machines are broadly categorized into **shared-memory MIMD** and **distributed-memory MIMD** based on the way PEs are coupled to the main memory.