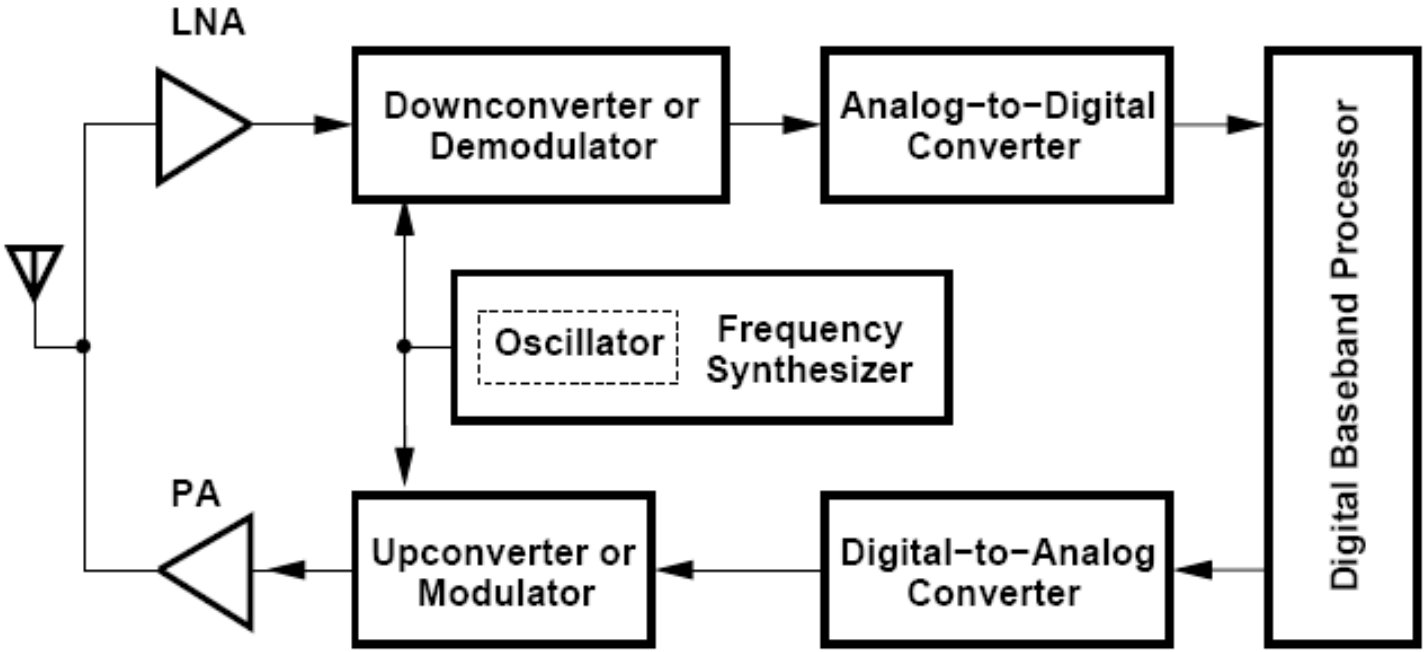
Voltage Controlled Oscillators

Προηγμένα Μικτά αναλογικά /ψηφιακά κυκλώματα και διατάξεις

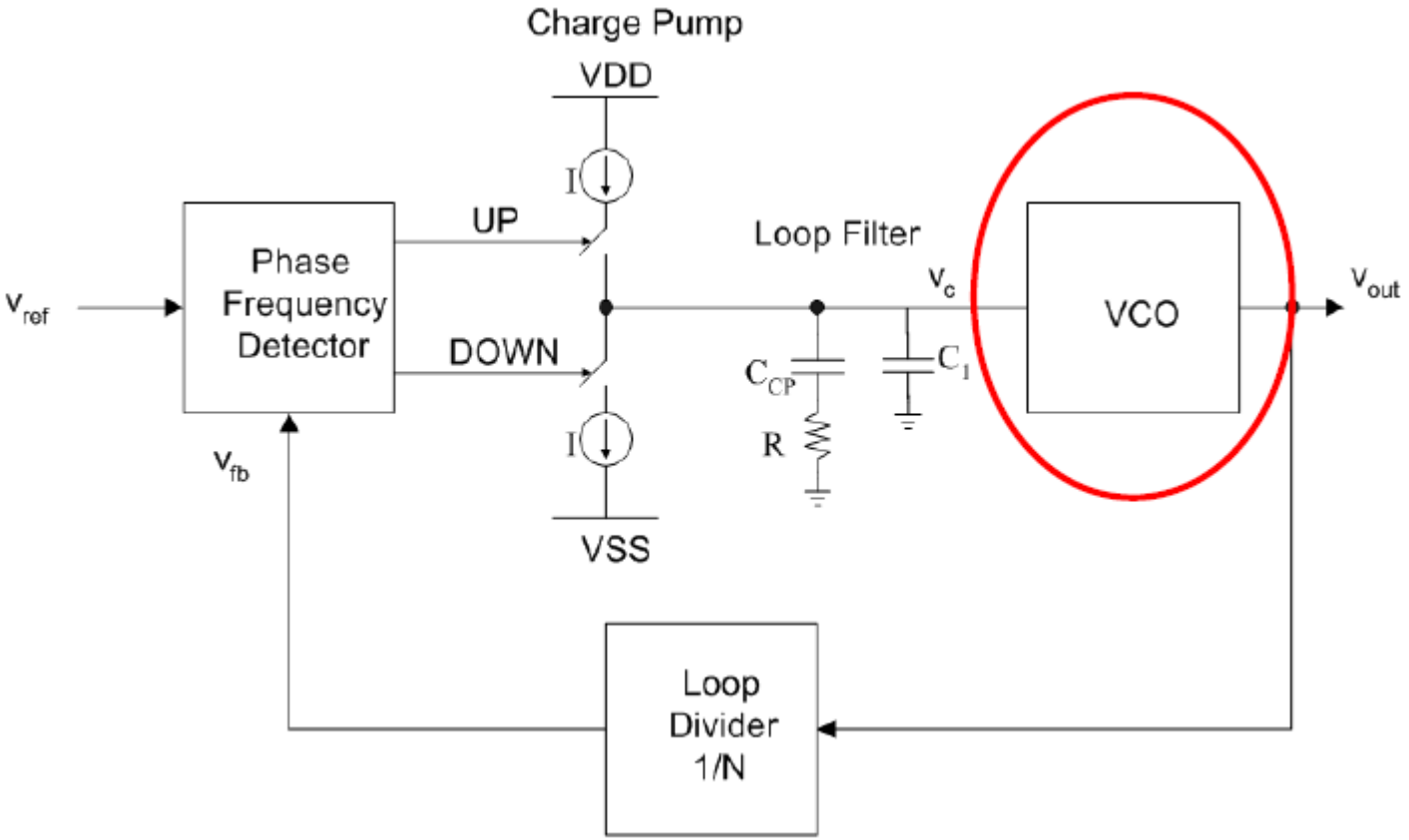
Varactors

- Varactor = voltage dependent capacitor
- Important properties:
  - capacitance range (vs. voltage)
  - quality factor (parasitic series resistance)
- Two ways to implement on an IC:
  - pn-junction (reverse-biased) - older technologies
  - MOSFET transistor - today

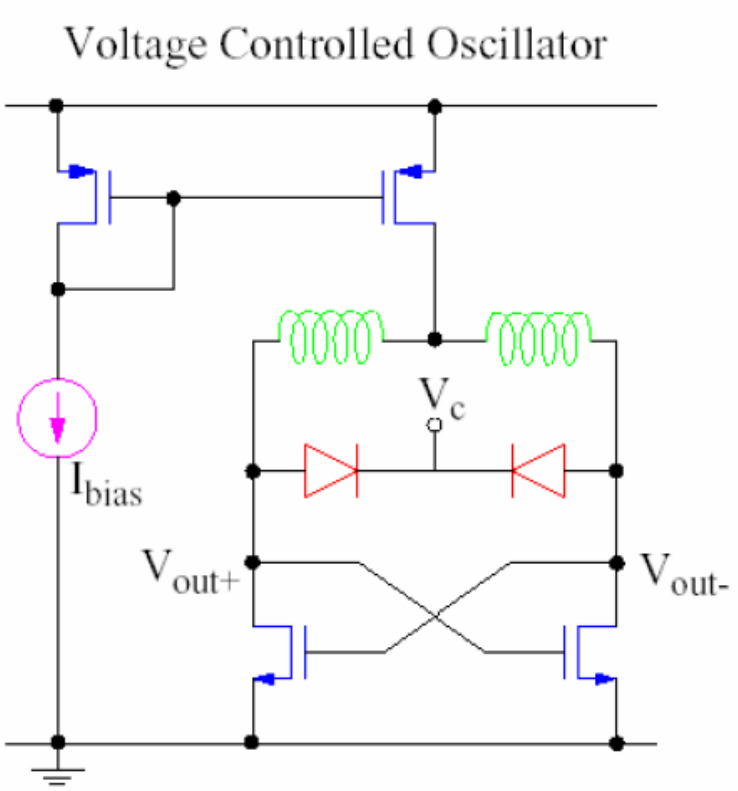
Πομποδέκτης RF



Synthesizer/ Phase –locked loop



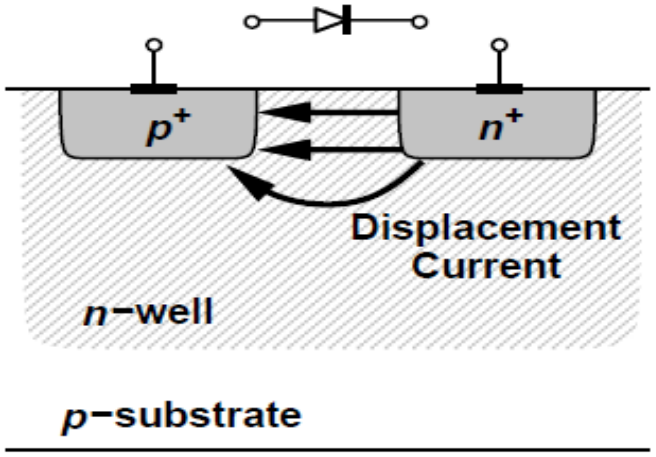
Στόχοι σχεδίασης VCO



- Phase noise, $L\{\Delta f\} = K_0 \left(\frac{f_0}{\Delta f}\right)^2 \left(\frac{1}{PQ}\right)$
  P: Output Power
  Q: Q-factor of the LC tank

- Maximize Q of the **inductor** and **varactor**
  Low phase-noise on-chip synthesizer
  Wide frequency tuning range
  Low power consumption(voltage supply)

Varactor Q Calculation Issues



Current distribution in varactor

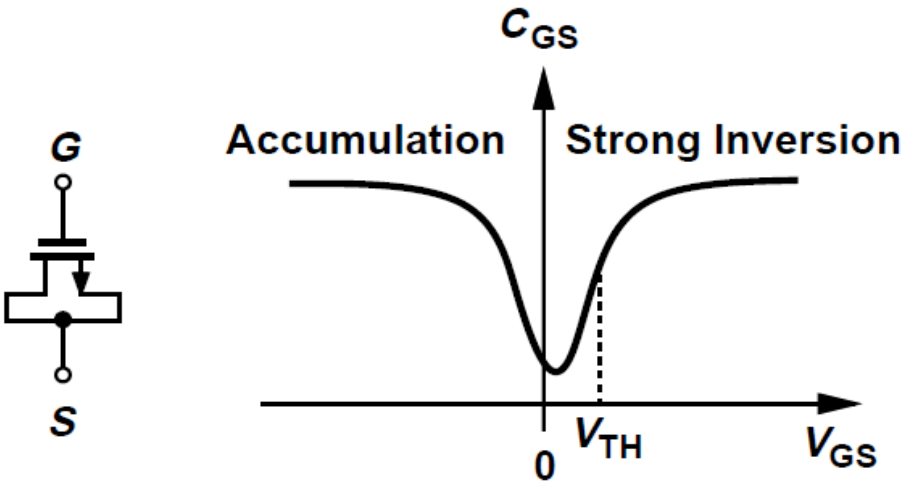
Q of varactor is obtained by measurement on fabricated structure

Difficult to calculate it

- **As shown above, due to the two dimensional flow of current it is difficult to compute the equivalent series resistance of the structure.**
- **N-well sheet resistance can not be directly applied to calculation of varactor series resistance.**

MOS Varactor ?

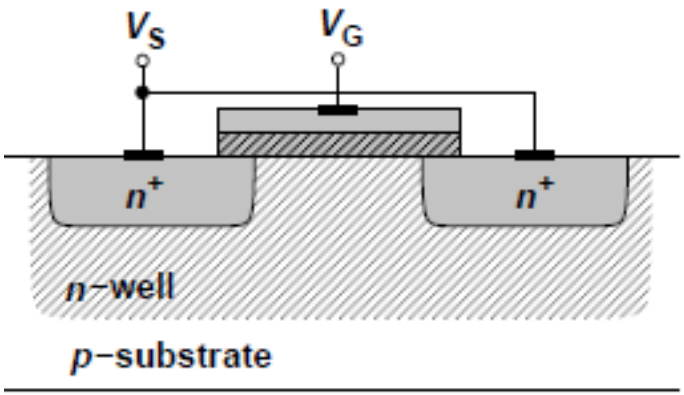
Regular MOS device:

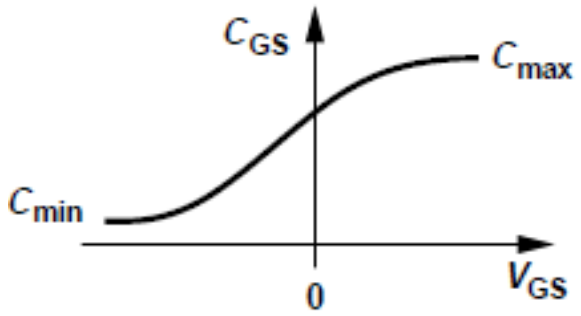


Variation of gate capacitance with Vgs

- **A regular MOSFET exhibits a voltage dependent gate capacitance**
- **The non-monotonic behavior with respect to gate voltage limits the design flexibility.**

Accumulation Mode MOS Varactor

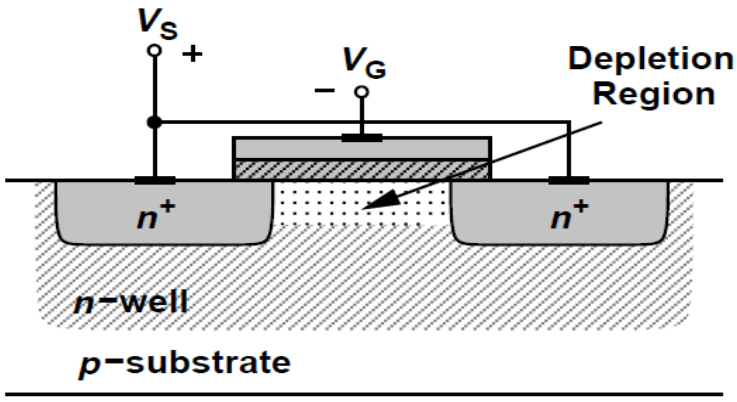




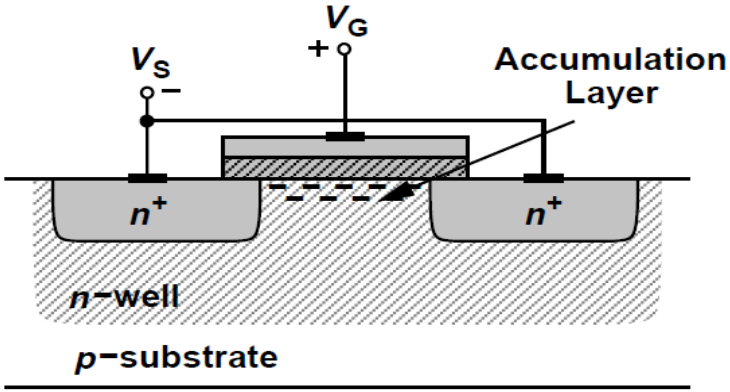
C/V characteristics of varactor

- Accumulation-mode MOS varactor is obtained by placing an NMOS inside an nwell .
- The variation of capacitance with Vgs is monotonic.
- The C/V characteristics scale well with scaling in technology.
- Unlike PN junction varactor this structure can operate with positive and negative bias so as to provide maximum tuning range.

Accumulation Mode MOS Varactor Operation



- Vg < Vs
- Depletion region is formed under gate oxide.
- Equivalent capacitance is the series combination of gate capacitance and depletion capacitance.



- Vg > Vs
- Formation of channel under gate oxide.

Accumulation Mode MOS Varactor: Curve Fitting Model

Curve fitting model:

$$C_{var}(V_{GS}) = \frac{C_{max} - C_{min}}{2} \tanh\left(a + \frac{V_{GS}}{V_0}\right) + \frac{C_{max} + C_{min}}{2}$$

Here, "V_o" and "a" allow fitting for the slope and the intercept.

- **The above varactor model translates to different characteristics in different circuit simulators.**
- **Simulation tools (HSPICE) that analyze circuits in terms of voltages and currents interpret the above non-linear capacitance equation correctly.**

Accumulation Mode MOS Varactor: Charge Equation Model

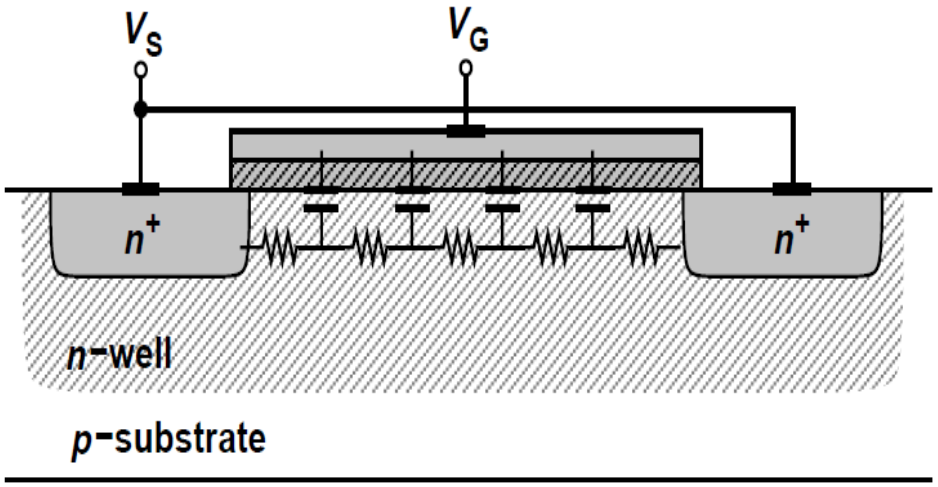
Charge equation model:

$$Q_{var} = \int C_{var}\, dV_{GS}$$

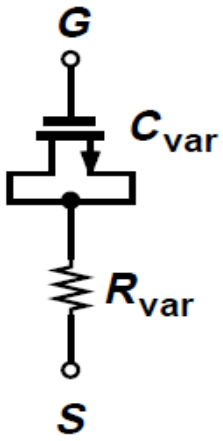
$$= \frac{C_{max} - C_{min}}{2} V_0 \ln\left[\cosh\left(a + \frac{V_{GS}}{V_0}\right)\right] + \frac{C_{max} + C_{min}}{2} V_{GS}$$

- **Simulation tools (Cadence Spectre) that represent the behavior of capacitors by charge equations interpret this charge equation model correctly.**

Q of Accumulation mode MOS Varactor



(a)

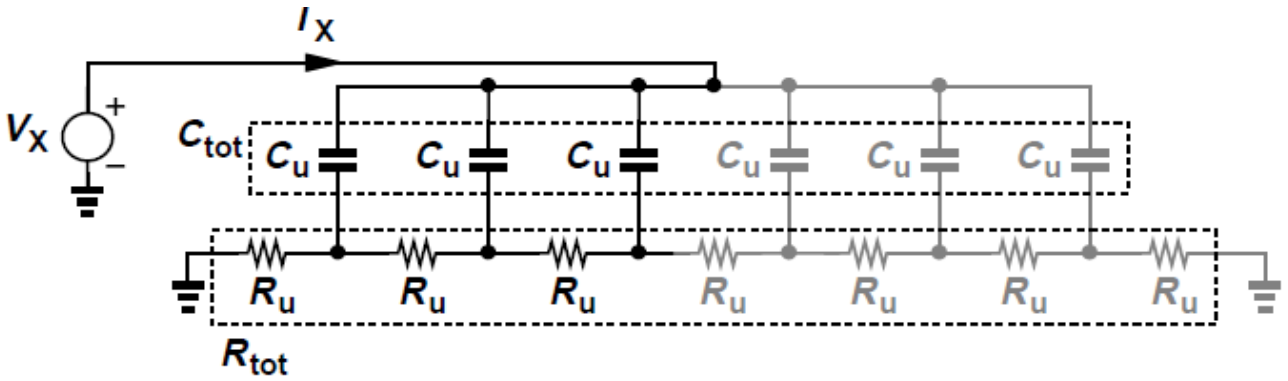


(b)

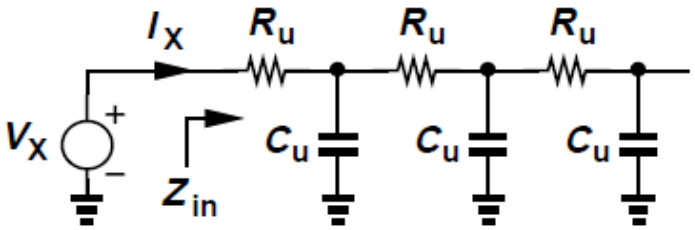
Q of varactor:

- **Determined by the resistance between source and drain terminals.**
- **Approximately calculated by lumped model shown in above.**

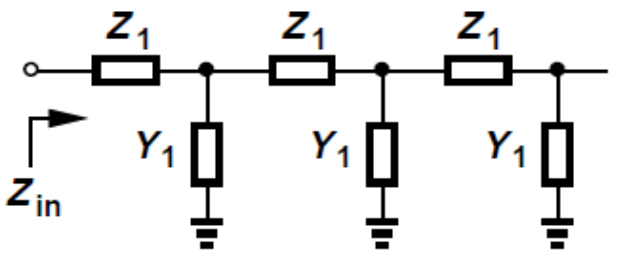
Calculation of Equivalent Resistance and Capacitance Value in Lumped Model.



Distributed Model



Equivalent structure for half circuit



Canonical T-line Structure

The equivalent structure above resembles a transmission line consisting of series resistances and parallel capacitances. For general T-line structure the input impedance is :

$$Z_{in} = \sqrt{\frac{Z_1}{Y_1}} \frac{1}{\tanh(\sqrt{Z_1 Y_1} d)}$$

Calculation of Equivalent Resistance and Capacitance Value in Lumped Model

Where Z_1 and Y_1 are specified for unit length and d is the length of line and from above equivalent structure $Z_1 d = R_{tot}$ and $Y_1 d = sC_{tot}$.

At frequencies well below $1/(R_{tot}C_{tot}/4)$, the argument of tanh is much less than unity, allowing the approximation,

$$\tanh \varepsilon = \varepsilon - \varepsilon^3/3$$

$$= \varepsilon/(1+\varepsilon^2/3)$$

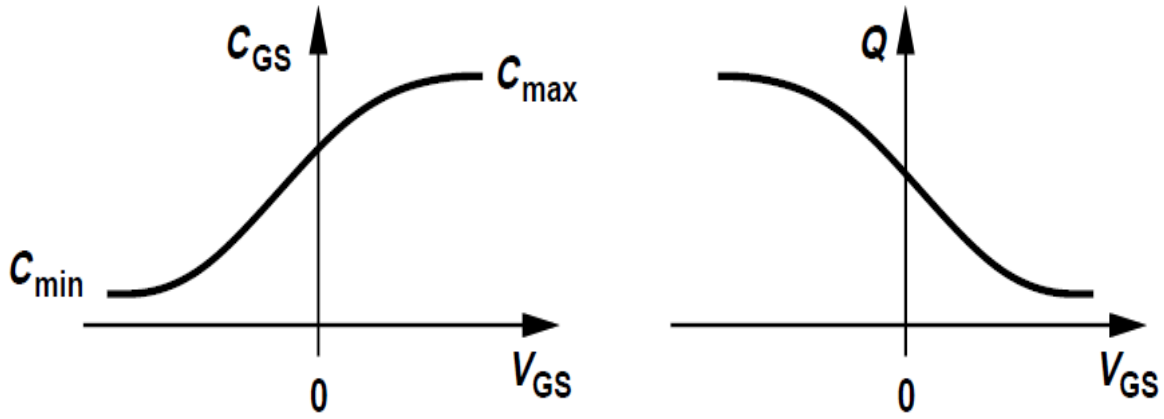
It follows that

$$Z_{in} \approx \frac{1}{C_{tot}s/2} + \frac{R_{tot}/2}{3}$$

The lumped model of half of the structure consists of its distributed capacitance in series with 1/3 of its distributed resistance. Accounting for the gray half in equivalent circuit of half structure, we obtain

$$Z_{in,tot} \approx \frac{1}{C_{tot}s} + \frac{R_{tot}}{12}$$

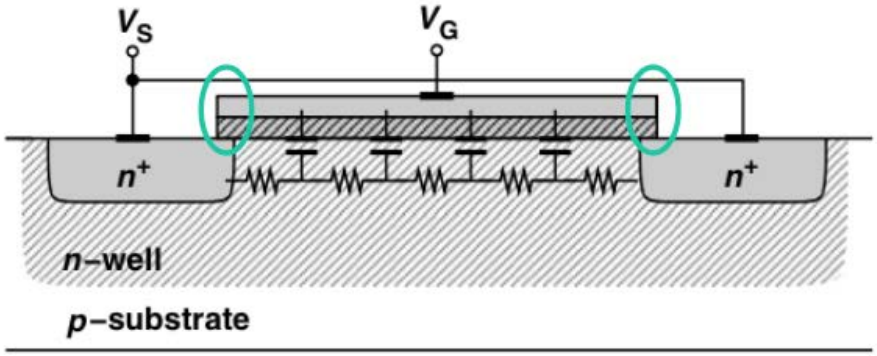
Variation of MOS Varactor Q with Capacitance

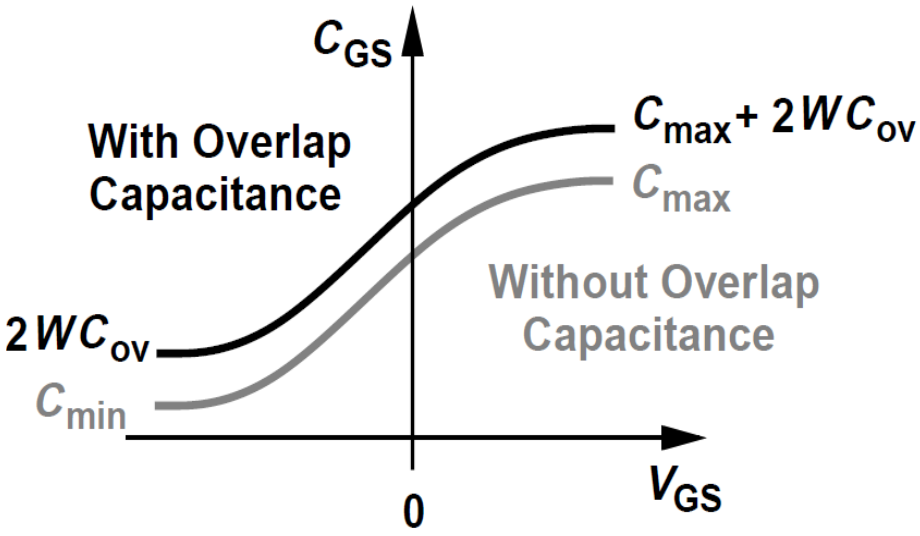


Variation of varactor Q with capacitance

- **For Cmin, the capacitance is small and resistance is large.**
- **For Cmax, the capacitance is large and resistance is small.**
- **Above comments suggest that Q remains relatively constant.**
- **In practice, Q drops as we increase cap from Cmin to Cmax, suggesting that relative rise in capacitance is greater than fall in resistance.**

Effect of Overlap Capacitance on Capacitance Range





- **Overlap capacitance is relatively voltage independent.**
- **Overlap capacitance shifts the C/V characteristics up, yielding a ratio of**

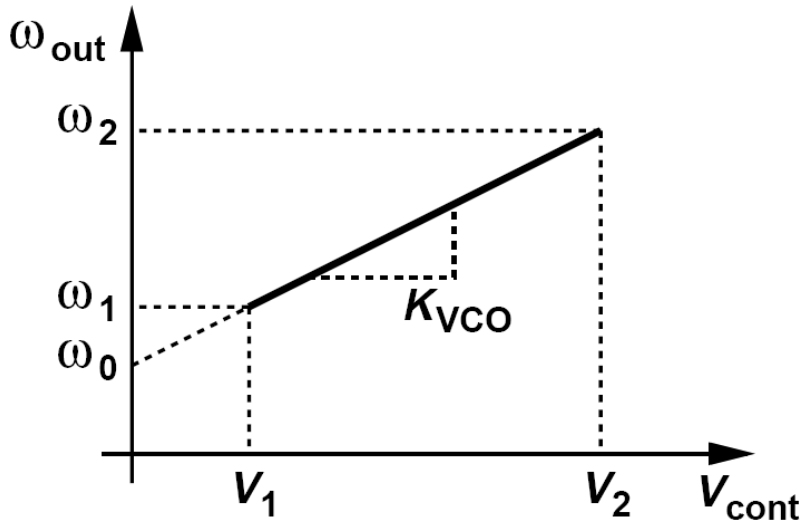
$$(C_{max} + 2WC_{ov})/(C_{min} + 2WC_{ov})$$

Example

- A MOS varactor realized in 65-nm technology has an effective length of 50 nm and a C_{ov} of 0.09 fF/μm. If C_{ox} = 17 fF/μm², determine the largest capacitance range that the varactor can provide.

Assuming a width of 1 μm for the device, we have $2WC_{ov} = 0.18$ fF and a gate oxide capacitance of $17\ \text{fF}/\mu\text{m}^2 \times 1\ \mu\text{m} \times 50\ \text{nm} = 0.85$ fF. Thus, the minimum capacitance is 0.18 fF (if the series combination of the oxide and depletion capacitances is neglected), and the maximum capacitance reaches 0.85 fF + 0.18 fF = 1.03 fF. The largest possible capacitance ratio is therefore equal to 5.72. In practice, the series combination of the oxide and depletion capacitances is comparable to $2WC_{ov}$, reducing this ratio to about 2.5.

Voltage-Controlled Oscillators: Characteristic



$$\omega_{out} = K_{VCO} V_{cont} + \omega_0$$

- The output frequency varies from ω_1 to ω_2 (the required tuning range) as the control voltage, V_{cont}, goes from V_1 to V_2.
- The slope of the characteristic, K_{VCO}, is called the "gain" or "sensitivity" of the VCO and expressed in rad/Hz/V.

Example: V_{DD} as the "Control Voltage"

As explained in previous example, the cross-coupled oscillator exhibits sensitivity to V_{DD}. Considering V_{DD} as the "control voltage," determine the gain.

If C_1 includes all circuit capacitances except C_{DB}

$$\omega_{osc} = \frac{1}{\sqrt{L_1(C_1 + C_{DB})}}$$

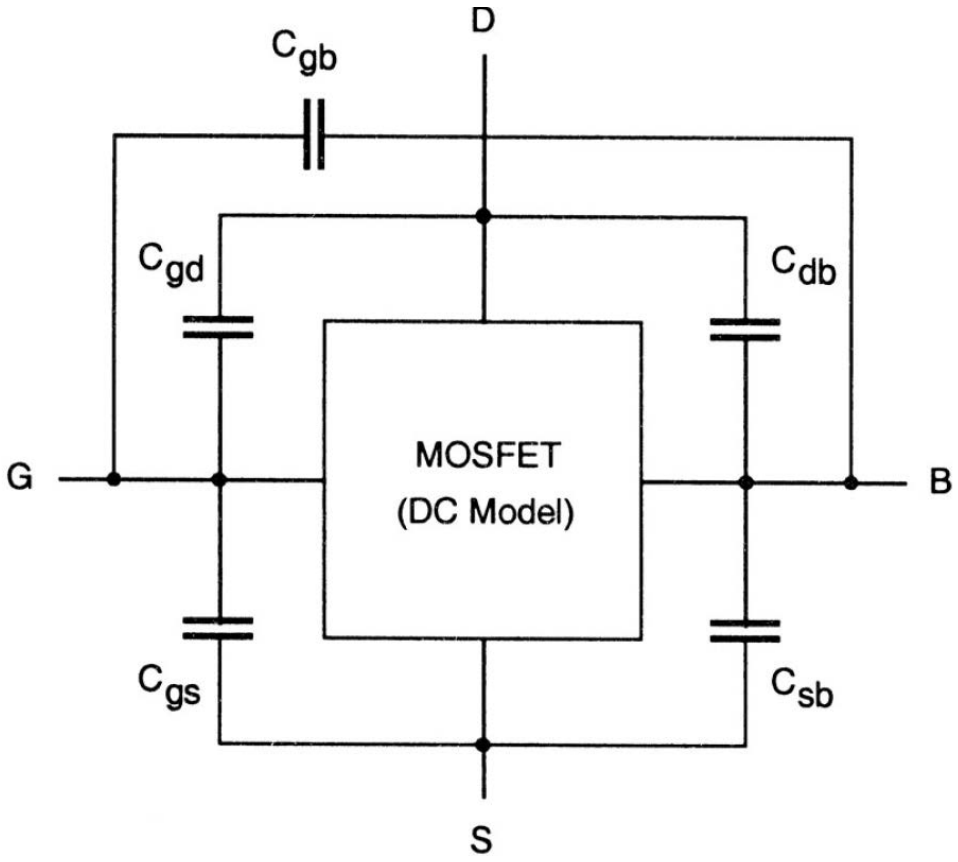
$$\begin{aligned} K_{VCO} &= \frac{\partial \omega_{out}}{\partial V_{DD}} \\ &= \frac{\partial \omega_{osc}}{\partial C_{DB}} \cdot \frac{\partial C_{DB}}{\partial V_{DD}} \end{aligned}$$

The junction capacitance is approximated as

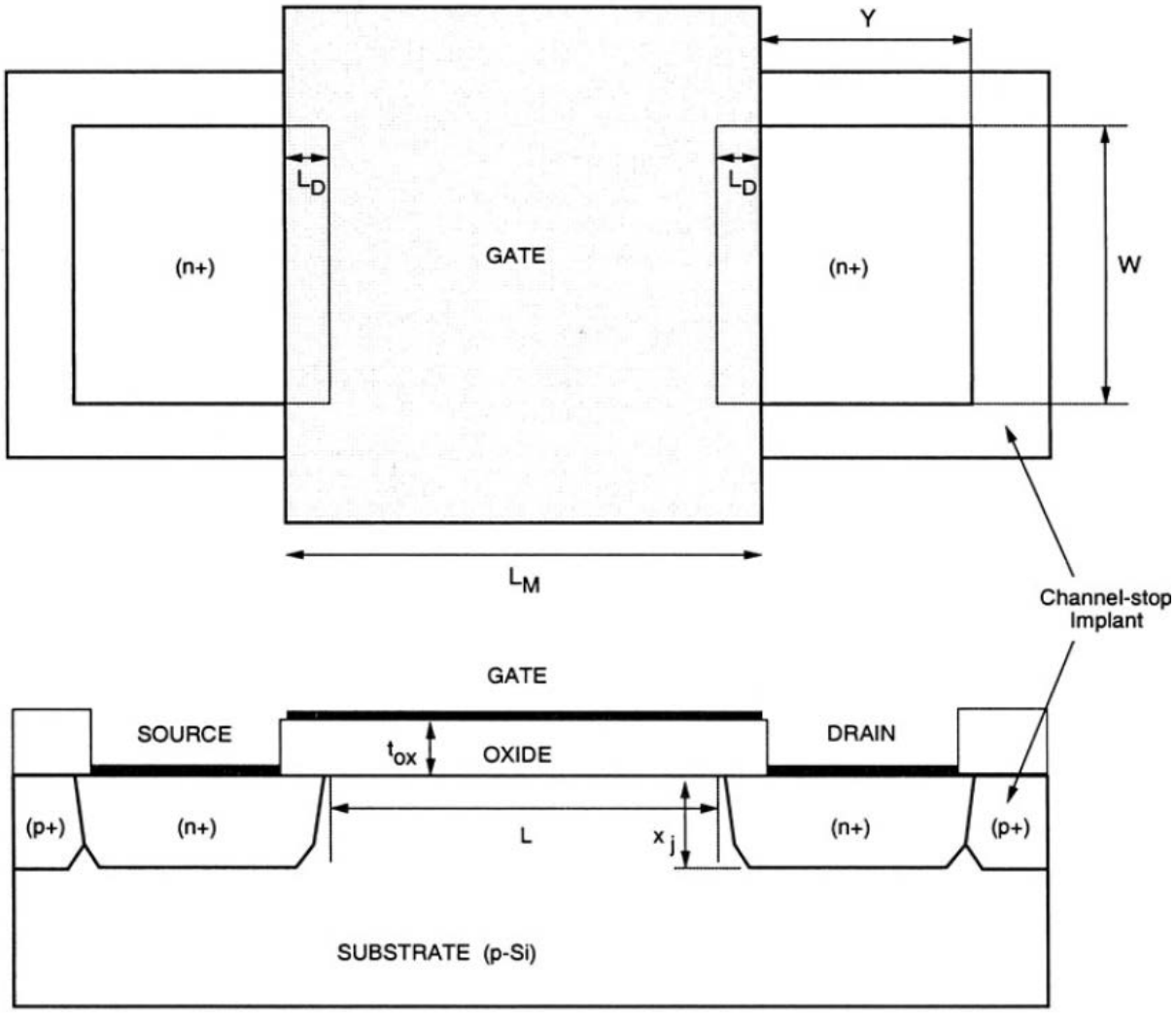
$$C_{DB} = \frac{C_{DB0}}{\left(1 + \frac{V_{DD}}{\phi_B}\right)^m}$$

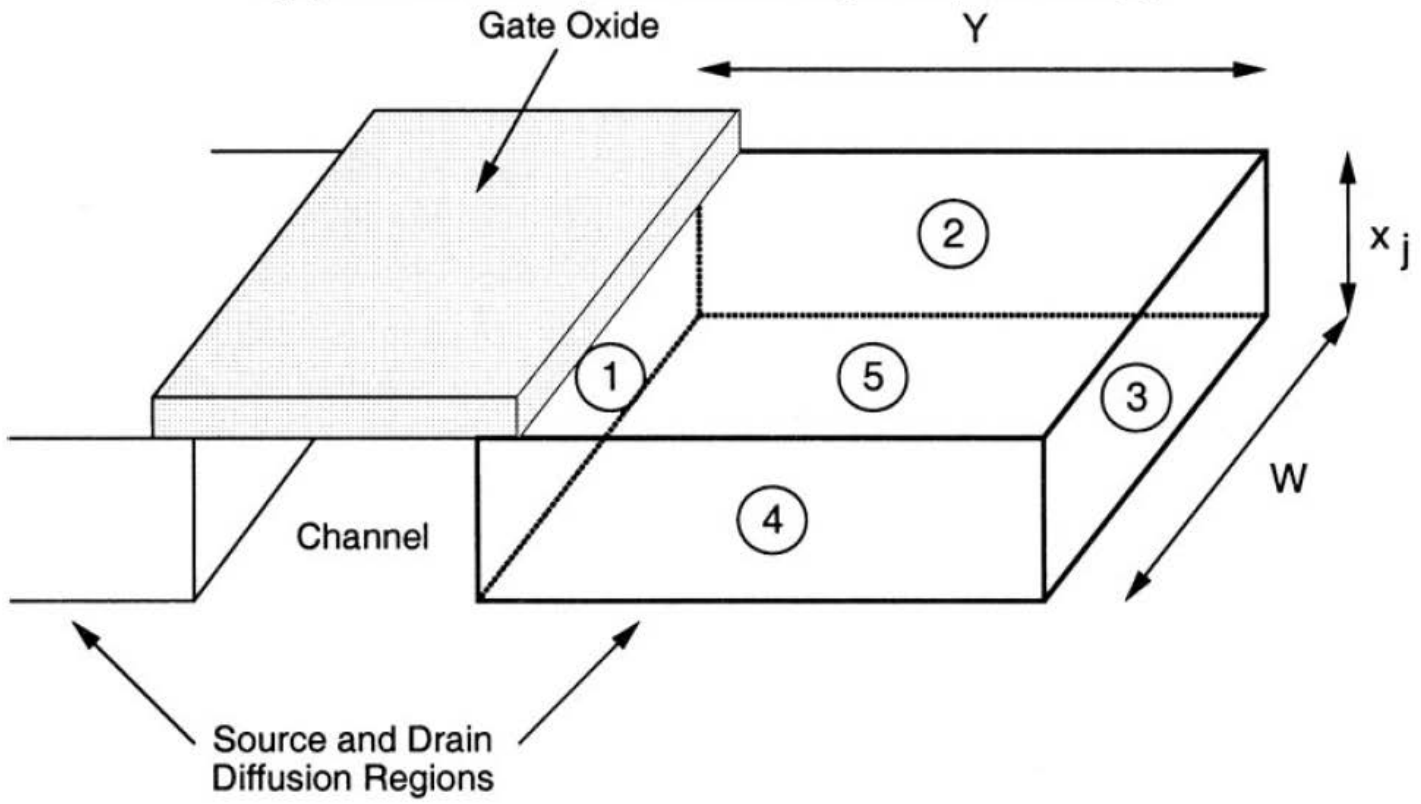
$$\begin{aligned} K_{VCO} &= \frac{-1}{2\sqrt{L_1}} \cdot \frac{1}{\sqrt{C_1 + C_{DB}}(C_1 + C_{DB})} \cdot \frac{-mC_{DB0}}{\phi_B \left(1 + \frac{V_{DD}}{\phi_B}\right)^{m+1}} \\ &= \frac{C_{DB}}{C_1 + C_{DB}} \cdot \frac{m}{2\phi_B + 2V_{DD}} \omega_{osc}. \end{aligned}$$

Χωρητικότητες MOSFET



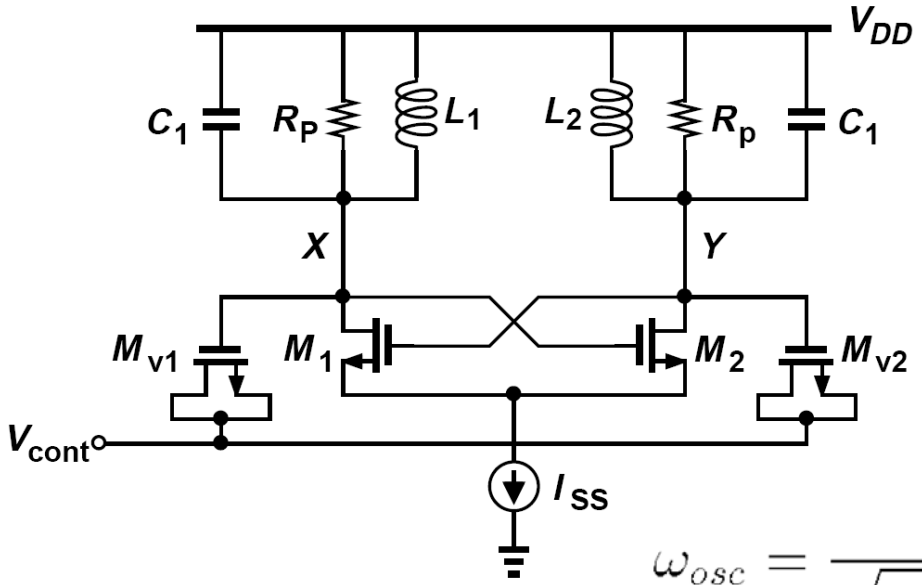
MOSFET Layout

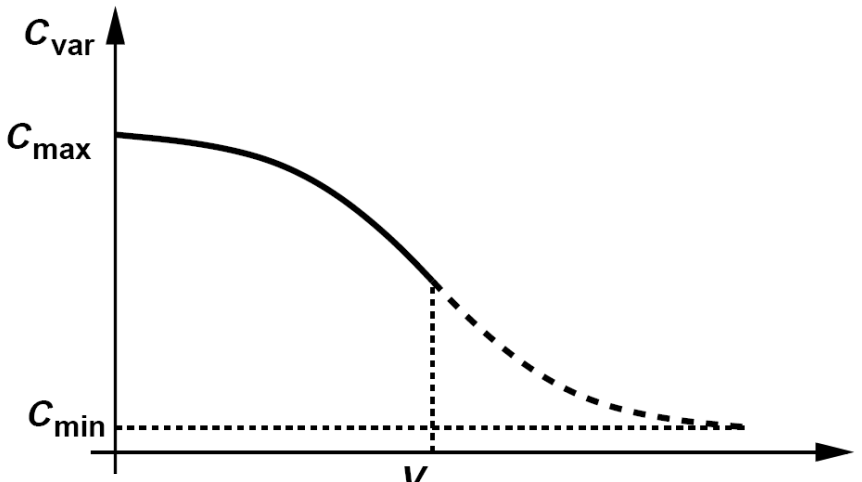




VCO Using MOS Varactors

- Since it is difficult to vary the inductance electronically, we only vary the capacitance by means of a varactor.
- MOS varactors are more commonly used than *pn* junctions, especially in low-voltage design.



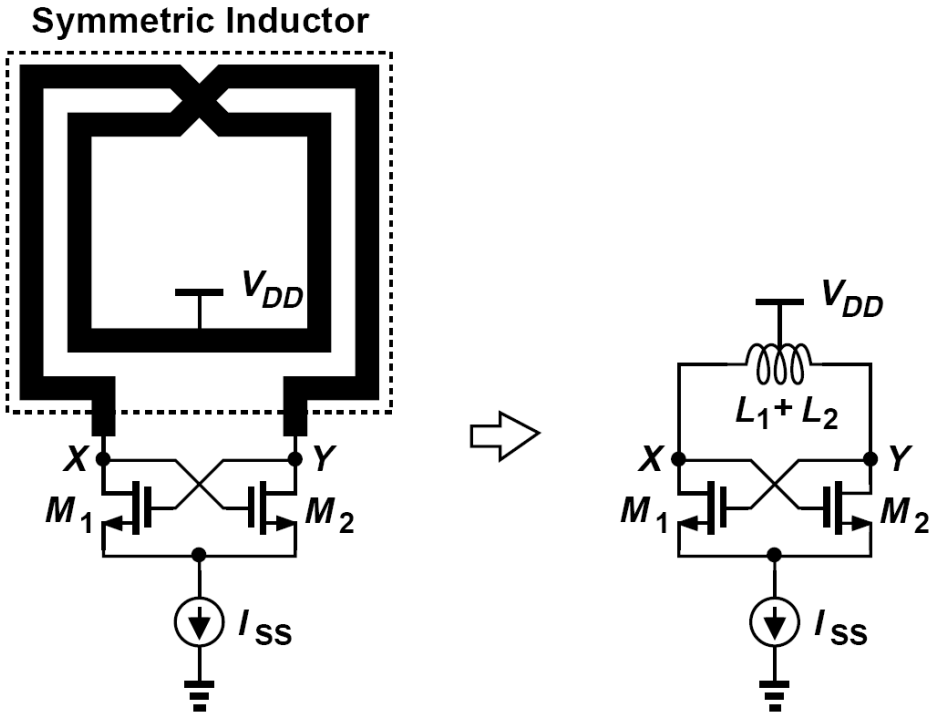


$$\omega_{osc} = \frac{1}{\sqrt{L_1(C_1 + C_{var})}}$$

- First, the varactors are stressed for part of the period if V_{cont} is near ground and V_X (or V_Y) rises significantly above V_{DD}.
- Second, only about half of C_{max} - C_{min} is utilized in the tuning.

Oscillator Using Symmetric Inductor

- **Symmetric spiral inductors excited by differential waveforms exhibit a higher *Q* than their single-ended counterparts.**



The symmetric inductor above has a value of 2 nH and a *Q* of 10 at 10 GHz. What is the minimum required transconductance of M_1 and M_2 to guarantee start-up?

$$g_{m1,2} \geq (630\ \Omega)^{-1}$$

Tuning Range Limitations

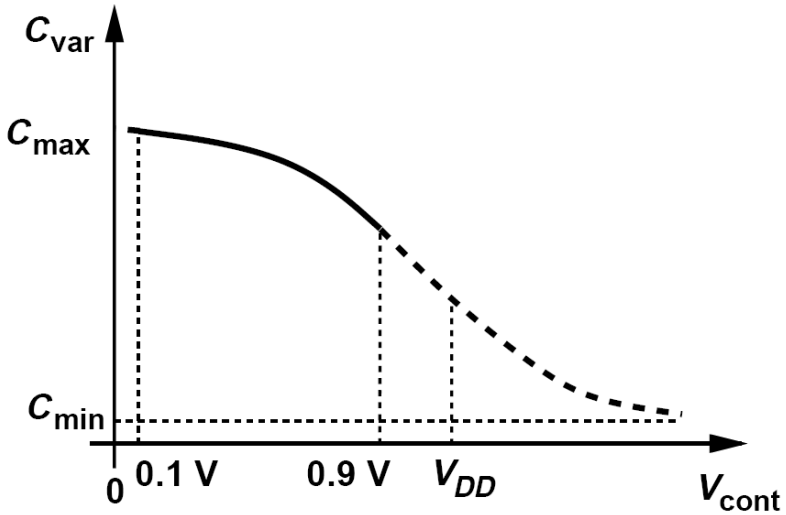
We make a crude approximation, $C_{var} << C_1$, and

$$\omega_{osc} \approx \frac{1}{\sqrt{L_1 C_1}} \left(1 - \frac{C_{var}}{2C_1}\right)$$

If the varactor capacitance varies from C_{var1} to C_{var2}, then the tuning range is given by

$$\Delta\omega_{osc} \approx \frac{1}{\sqrt{L_1 C_1}} \frac{C_{var2} - C_{var1}}{2C_1}$$

- **The tuning range trades with the overall tank *Q*.**
- **Another limitation on C_{var2} - C_{var1} arises from the available range for the control voltage of the oscillator, V_{cont}.**

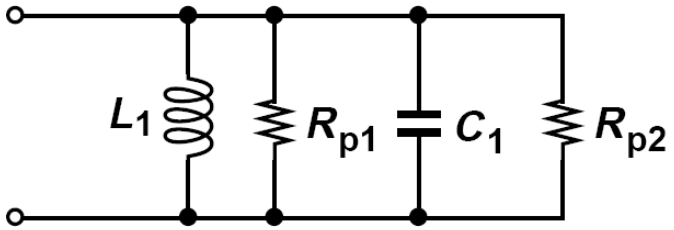


Effect of Varactor *Q:* Tank Consisting of Lossy Inductor and Capacitor

A lossy inductor and a lossy capacitor form a parallel tank. Determine the overall *Q* in terms of the quality factor of each.

The loss of an inductor or a capacitor can be modeled by a parallel resistance (for a narrow frequency range). We therefore construct the tank as shown below, where the inductor and capacitor *Q*'s are respectively given by:

$$Q_L = \frac{R_{p1}}{L_1\omega}$$
$$Q_C = R_{p2}C_1\omega$$



Merging R_{p1} and R_{p2} yields the overall *Q*:

$$Q_{tot} = \frac{R_{p1}R_{p2}}{R_{p1}+R_{p2}} \cdot \frac{1}{L_1\omega}$$
$$= \frac{1}{\frac{L_1\omega}{R_{p1}} + \frac{L_1\omega}{R_{p2}}}$$
$$= \frac{1}{\frac{L_1\omega}{R_{p1}} + \frac{1}{R_{p2}C_1\omega}}.$$

$$\Rightarrow \quad \frac{1}{Q_{tot}} = \frac{1}{Q_L} + \frac{1}{Q_C}$$

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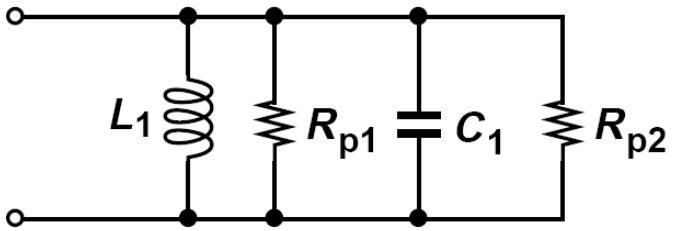
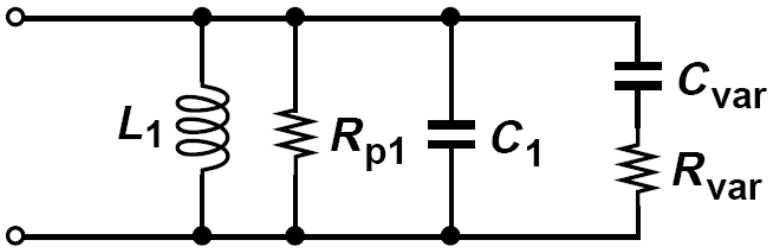


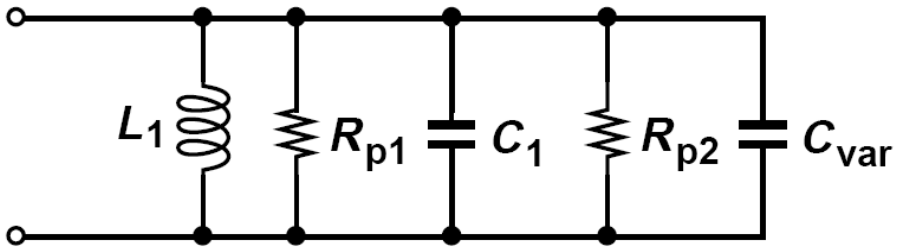
Merging R_{p1} and R_{p2} yields the overall *Q*:

$$Q_{tot} = \frac{R_{p1}R_{p2}}{R_{p1}+R_{p2}} \cdot \frac{1}{L_1\omega}$$
$$= \frac{1}{\frac{L_1\omega}{R_{p1}} + \frac{L_1\omega}{R_{p2}}}$$
$$= \frac{1}{\frac{L_1\omega}{R_{p1}} + \frac{1}{R_{p2}C_1\omega}}.$$

$$\Rightarrow \quad \frac{1}{Q_{tot}} = \frac{1}{Q_L} + \frac{1}{Q_C}$$

Tank Using Lossy Varactor





Transforming the series combination of C_{var} and R_{var} to a parallel combination

$$R_{p2} = \frac{1}{C_{var}^2 \omega^2 R_{var}}$$

The *Q* associated with C_1+C_{var} is equal to

$$\begin{aligned} Q_C &= R_{P2}(C_1 + C_{var})\omega \\ &= \frac{C_1 + C_{var}}{C_{var}^2 \omega R_{var}}. \end{aligned}$$

$$Q_C = \left(1 + \frac{C_1}{C_{var}}\right) Q_{var}$$

The overall tank Q is therefore given by

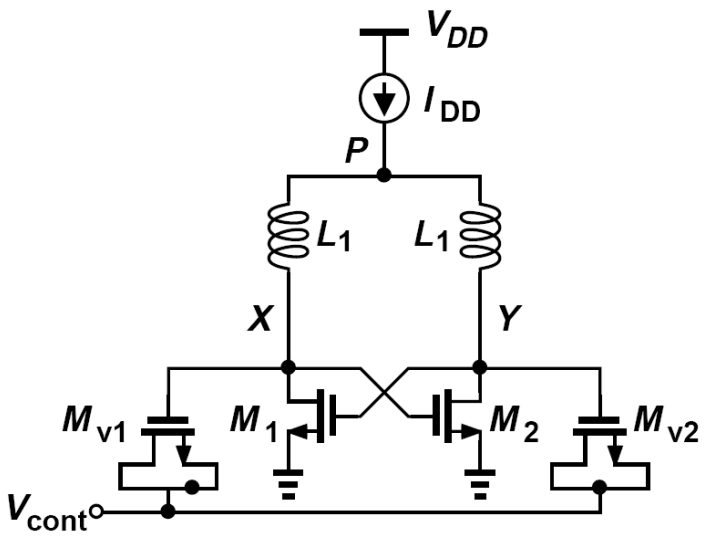
$$\frac{1}{Q_{tot}} = \frac{1}{Q_L} + \frac{1}{\left(1 + \frac{C_1}{C_{var}}\right) Q_{var}}$$

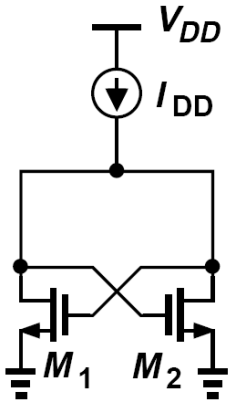
Equation above can be generalized if the tank consists of an ideal capacitor, C_1, and lossy capacitors, C_2-C_n, that exhibit a series resistance of R_2-R_n, respectively.

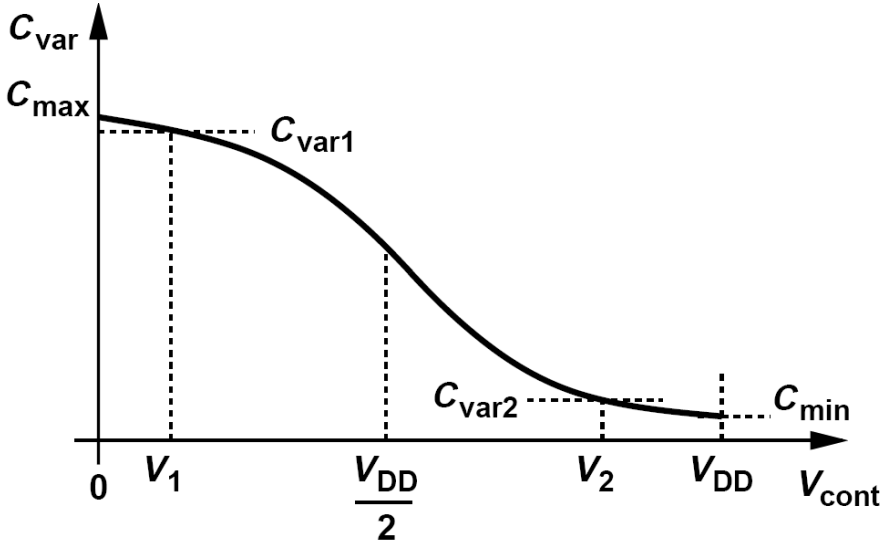
$$\frac{1}{Q_{tot}} = \frac{1}{Q_L} + \frac{C_2}{C_{tot}}\frac{1}{Q_2} + \cdots + \frac{C_n}{C_{tot}}\frac{1}{Q_n}$$

LC VCOs with Wide Tuning Range: VCOs with Continuous Tuning

- **We seek oscillator topologies that allow both positive and negative (average) voltages across the varactors, utilizing almost the entire range from C_{min} to C_{max}.**







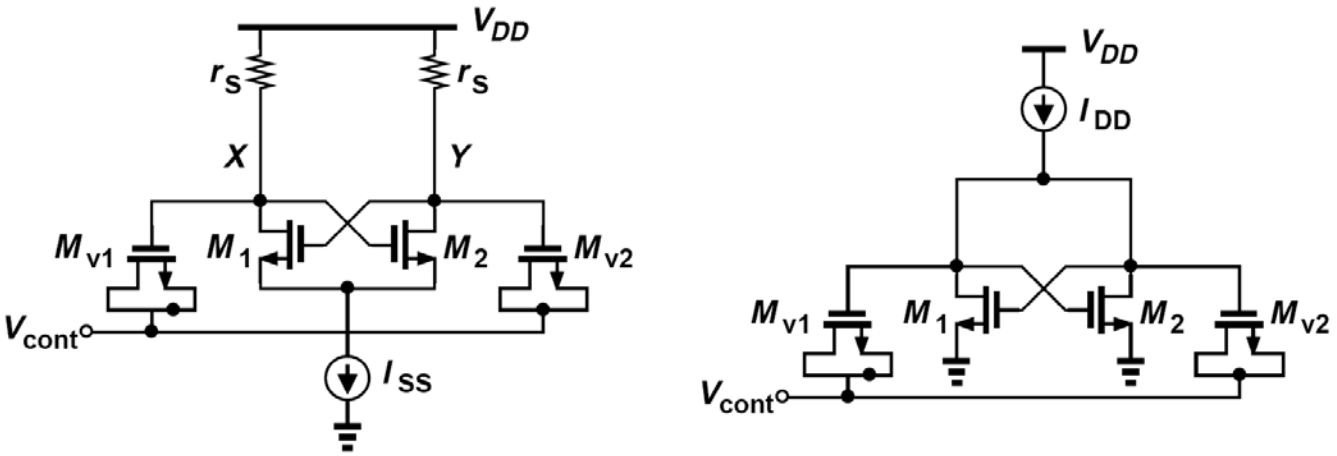
The CM level is simply given by the gate-source voltage of a diode-connected transistor carrying a current of $I_{DD}/2$.

$$V_{GS1,2} = \sqrt{\frac{I_{DD}}{\mu_n C_{ox}(W/L)}} + V_{TH}$$

We select the transistor dimensions such that the CM level is approximately equal to $V_{DD}/2$. Consequently, as V_{cont} varies from 0 to V_{DD}, the gate-source voltage of the varactors, $V_{GS,var}$, goes from $+V_{DD}/2$ to $-V_{DD}/2$,

Output CM Dependence on Bias Current

The tail or top bias current in the above oscillators is changed by DI. Determine the change in the voltage across the varactors.



Each inductor contains a small low-frequency resistance, r_s . If I_{SS} changes by ΔI, the output CM level changes by $\Delta V_{CM} = (\Delta I/2) r_s$, and so does the voltage across each varactor. In the top-biased circuit, on the other hand, a change of ΔI flows through two diode-connected transistors, producing an output CM change of $\Delta V_{CM} = (\Delta I/2)(1/g_m)$. Since $1/g_m$ is typically in the range of a few hundred ohms, the top-biased topology suffers from a much higher varactor voltage modulation.

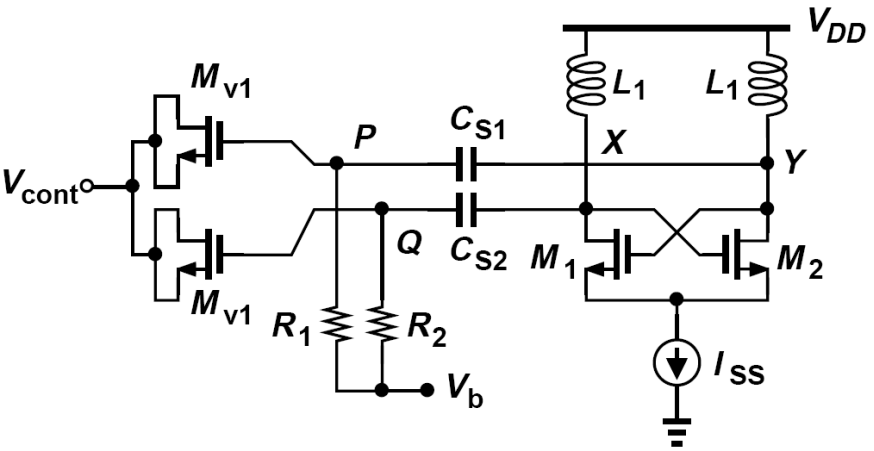
What is the change in the oscillation frequency in the above example?

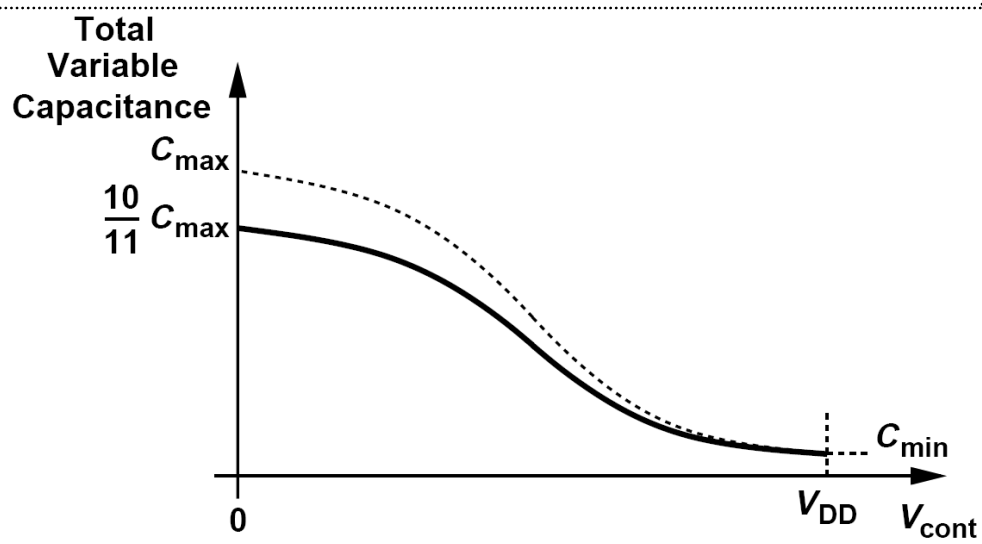
Since a CM change at *X* and *Y* is indistinguishable from a change in V_{cont}, we have

$$\begin{aligned} \Delta\omega &= K_{VCO}\Delta V_{CM} \\ &= K_{VCO}\frac{\Delta I}{2}r_s \quad \text{or} \quad K_{VCO}\frac{\Delta I}{2}\frac{1}{g_m} \end{aligned}$$

VCO Using Capacitor Coupling to Varactors

- **In order to avoid varactor modulation due to the noise of the bias current source, we return to the tail-biased topology but employ ac coupling between the varactors and the core so as to allow positive and negative voltages across the varactors.**



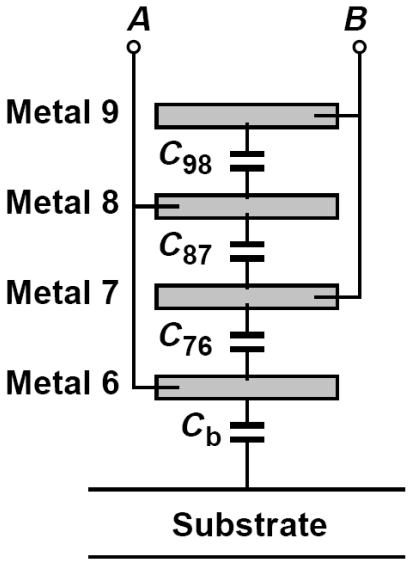


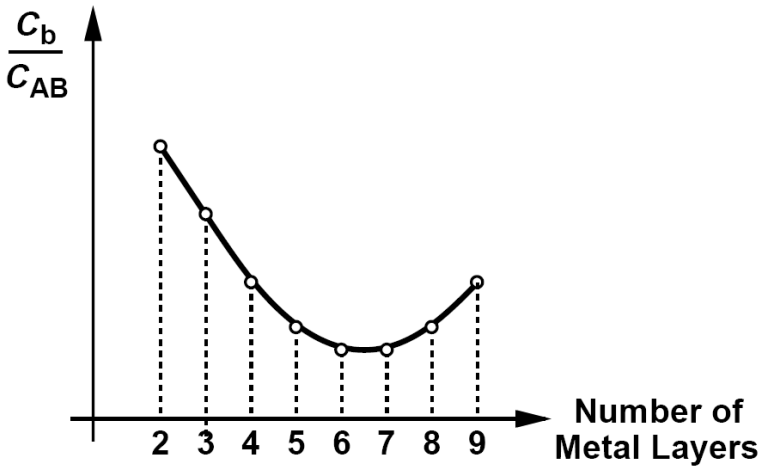
- **The principal drawback of the above circuit stems from the parasitics of the coupling capacitors.**

$$\Delta\omega_{os} \approx \frac{1}{\sqrt{L_1 C_1}} \cdot \frac{1}{2C_1} \cdot \frac{C_S^2 (C_{var2} - C_{var1})}{(C_S + C_{var2})(C_S + C_{var1})}$$

VCO Using Capacitor Coupling to Varactors: Parasitic Capacitances to the Substrate

- The choice of $C_S = 10C_{max}$ reduces the capacitance range by 10% but introduces substantial parasitic capacitances at X and Y or at P and Q because integrated capacitors suffer from parasitic capacitances to the substrate.





- C_b/C_{AB} typically exceeds 5%.

VCO Using Capacitor Coupling to Varactors: Effect of the Parasitics of C_{S1} and C_{S2}

- **A larger C_1 further limits the tuning range.**

$$\Delta\omega_{osc} \approx \frac{1}{\sqrt{L_1(C_1+0.5C_{max})}} \times \frac{1}{2(C_1+0.5C_{max})} \times \frac{C_S^2(C_{max}-0.5C_{max})}{(10C_{max}+C_{max})(10C_{max}+0.5C_{max})}$$

$$\approx \frac{1}{\sqrt{L_1(C_1+0.5C_{max})}} \times \frac{0.43C_{max}}{2(C_1+0.5C_{max})}.$$

The VCO above is designed for a tuning range of 10% without the series effect of C_S and parallel effect of C_b. If $C_S = 10C_{max}$, $C_{max} = 2C_{min}$, and $C_b = 0.05C_S$, determine the actual tuning range.

Without the effects of C_S and C_b $\Delta\omega_{osc} \approx \frac{1}{\sqrt{L_1C_1}} \frac{0.5C_{max}}{2C_1}$

For this range to reach 10% of the center frequency, we have $C_{max} = \frac{2}{5}C_1$

With the effects of C_S and C_b $\Delta\omega_{osc} \approx \frac{1}{\sqrt{L_1(1.2C_1)}} \times \frac{0.43}{6}$

$$\approx \frac{7.2\%}{\sqrt{1.2L_1C_1}}.$$

Figures of Merit of VCOs

- **Our studies in this chapter point to direct trade-offs among the phase noise, power dissipation, and tuning range of VCOs.**

A figure of merit (FOM) that encapsulates some of these trade-offs is defined as

$$\text{FOM}_1 = \frac{(\text{Oscillation Frequency})^2}{\text{Power Dissipation} \times \text{Phase Noise} \times (\text{Offset Frequency})^2}$$

Another FOM that additionally represents the trade-offs with the tuning range is

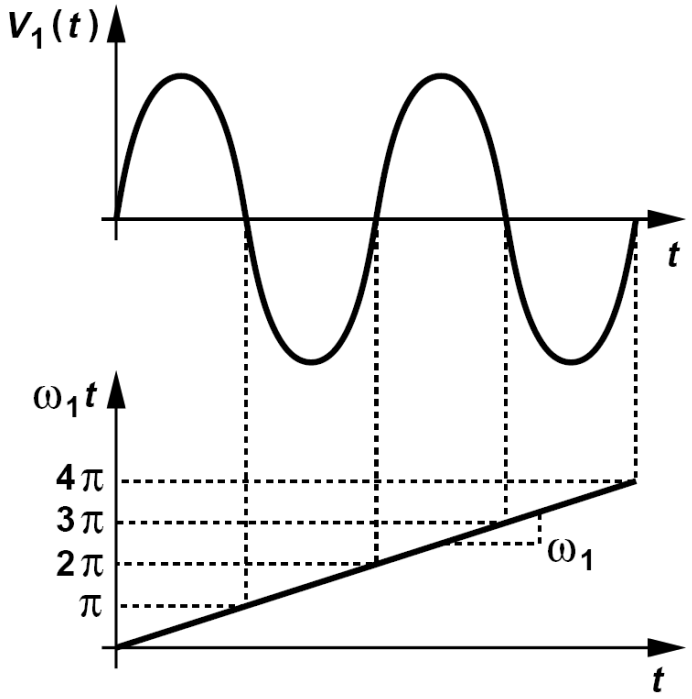
$$\text{FOM}_2 = \frac{(\text{Oscillation Frequency})^2}{\text{Power Dissipation} \times \text{Phase Noise} \times (\text{Offset Frequency})^2} \times \left(\frac{\text{Tuning Range}}{\text{Oscillation Frequency}}\right)^2$$

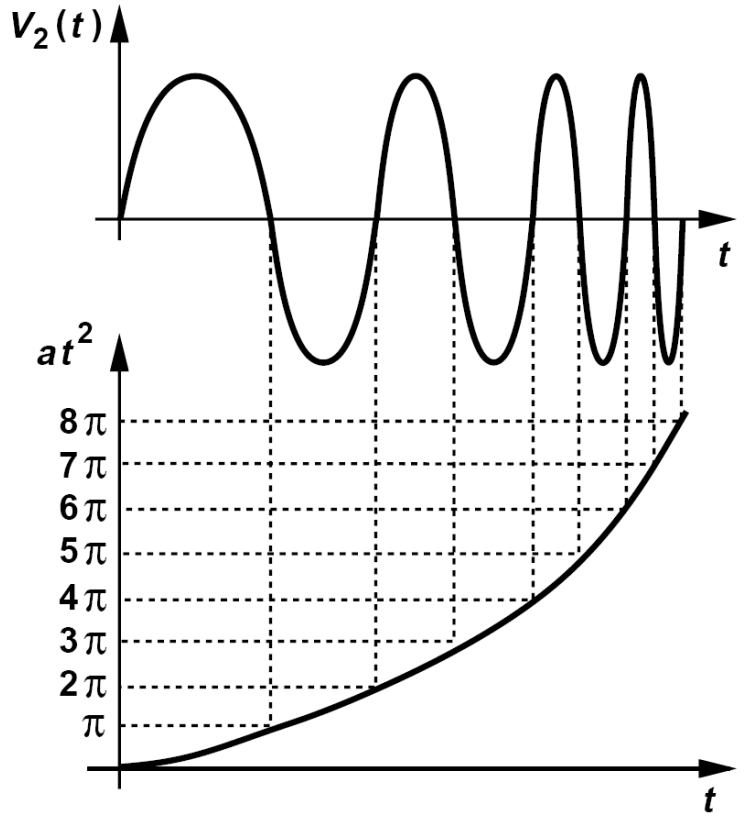
- **In general, the phase noise in the above expressions refers to the worst-case value, typically at the highest oscillation frequency.**
- **Also, note that these FOMs do not account for the load driven by the VCO.**

Mathematical Model of VCOs: Linear and Quadrature Growth of Phase with Time

Plot the waveforms for $V_1(t) = V_0 \sin\omega_1 t$ and $V_2(t) = V_0 \sin(at2)$.

To plot these waveforms carefully, we must determine the time instants at which the argument of the sine reaches integer multiples of π. For $V_1(t)$, the argument, $\omega_1 t$, rises linearly with time, crossing $k\pi$ at $t = \pi k/\omega_1$. For $V_2(t)$, on the other hand, the argument rises increasingly faster with time, crossing $k\pi$ more frequently.



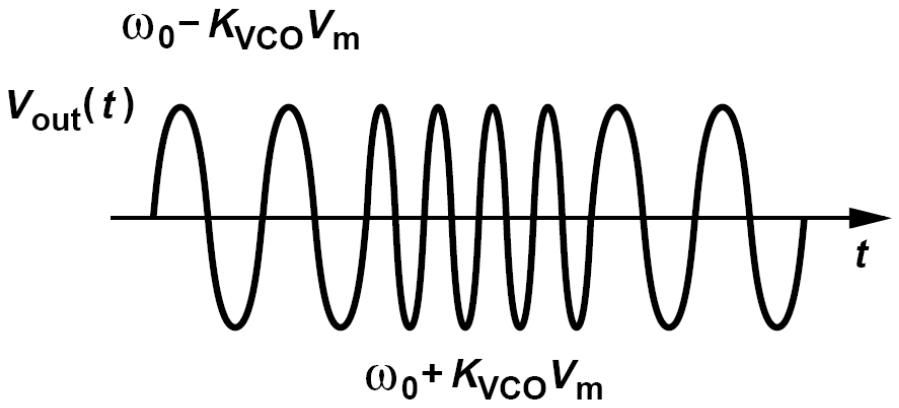


Example of Mathematical Model of VCOs (I)

Since a sinusoid of constant frequency !1 can be expressed as V0 cos !1t, a student surmises that the output waveform of a VCO can be written as

$$V_{out}(t) = V_0 \cos \omega_{out} t$$
$$= V_0 \cos(\omega_0 + K_{VCO} V_{cont})t$$

Explain why this is incorrect.

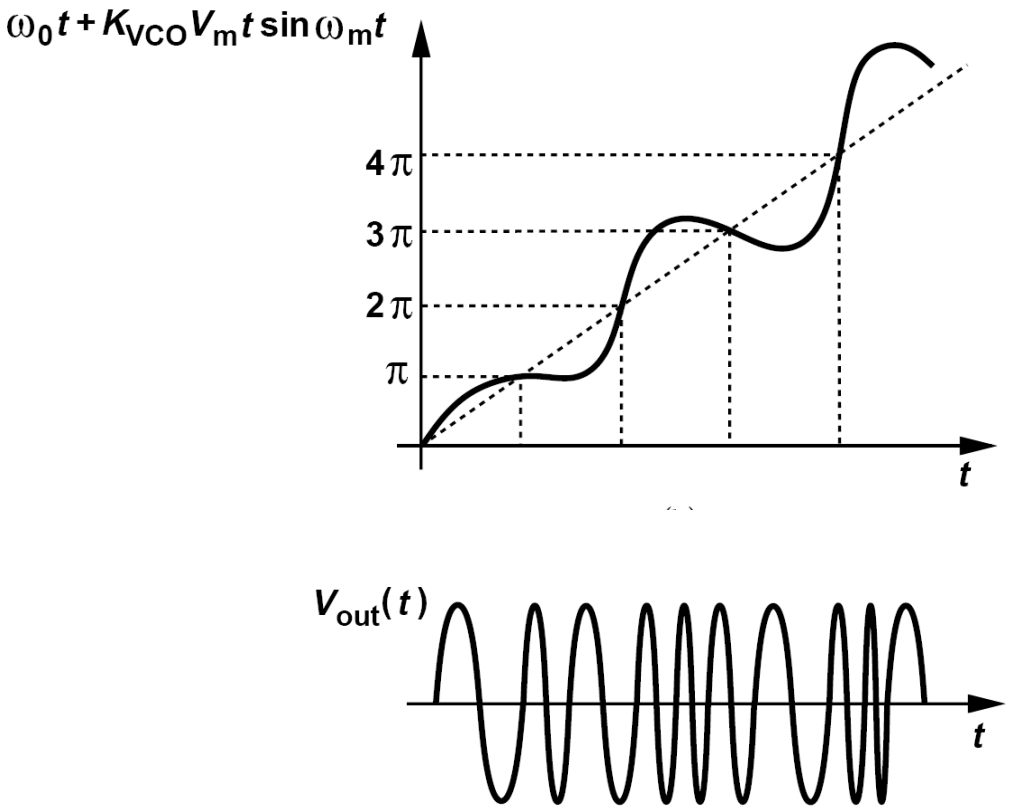


As an example, suppose $V_{cont} = V_m \sin \omega_m t$, i.e., the frequency of the oscillator is modulated periodically. Intuitively, we expect the output waveform frequency periodically swings between $\omega_0 + K_{VCO}V_m$ and $\omega_0 - K_{VCO}V_m$, i.e., has a "peak deviation" of $\pm K_{VCO}V_m$. However, the student's expression yields

$$V_{out}(t) = V_0 \cos[\omega_0 t + K_{VCO} V_m (\sin \omega_m t)t]$$

Example of Mathematical Model of VCOs (Ⅱ)

We plot the overall argument and draw horizontal lines corresponding to $k\pi$.



The intersection of each horizontal line with the phase plot signifies the zero crossings of $V_{out}(t)$. Thus, $V_{out}(t)$ appears as shown above. The key point here is that the VCO frequency is not modulated periodically.