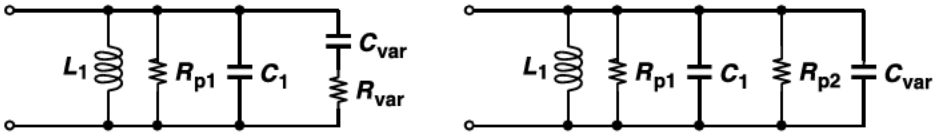

Figure 8.29 *(a) Tank using lossy varactor, (b) equivalent circuit.*

R_{var} to a parallel combination [Fig. 8.29(b)], we have from Chapter 2

$$R_{p2} = \frac{1}{C_{var}^2 \omega^2 R_{var}}. \tag{8.60}$$

To utilize our previous results, we combine C_1 and C_{var}. The Q associated with $C_1 + C_{var}$ is equal to

$$Q_C = R_{P2}(C_1 + C_{var})\omega \tag{8.61}$$

$$= \frac{C_1 + C_{var}}{C_{var}^2 \omega R_{var}}. \tag{8.62}$$

Recognizing that $Q_{var} = (C_{var}\omega R_{var})^{-1}$, we have

$$Q_C = \left(1 + \frac{C_1}{C_{var}}\right) Q_{var}. \tag{8.63}$$

In other words, the Q of the varactor is "boosted" by a factor of $1 + C_1/C_{var}$. The overall tank Q is therefore given by

$$\frac{1}{Q_{tot}} = \frac{1}{Q_L} + \frac{1}{\left(1 + \dfrac{C_1}{C_{var}}\right) Q_{var}}. \tag{8.64}$$

For frequencies as high as several tens of gigahertz, the first term in Eq. (8.64) is dominant (unless a long channel is chosen for the varactors).

Equation (8.64) can be generalized if the tank consists of an ideal capacitor, C_1, and lossy capacitors, C_2-C_n, that exhibit a series resistance of R_2-R_n, respectively. The reader can prove that

$$\frac{1}{Q_{tot}} = \frac{1}{Q_L} + \frac{C_2}{C_{tot}}\frac{1}{Q_2} + \cdots + \frac{C_n}{C_{tot}}\frac{1}{Q_n}, \tag{8.65}$$

where $C_{tot} = C_1 + \cdots + C_n$ and $Q_j = (R_j C_j \omega)^{-1}$.

8.6 LC VCOs WITH WIDE TUNING RANGE

8.6.1 VCOs with Continuous Tuning

The tuning range obtained from the C–V characteristic depicted in Fig. 8.27 may prove prohibitively narrow, particularly because the capacitance range corresponding to *negative*

V_{GS} (for $V_{cont} > V_{DD}$) remains unused. We must therefore seek oscillator topologies that allow both positive and negative (average) voltages across the varactors, utilizing almost the entire range from C_{min} to C_{max}.

Figure 8.30(a) shows one such topology. Unlike the tail-biased configuration studied in Section 8.3, this circuit defines the bias currents of M_1 and M_2 by a *top* current source, I_{DD}. We analyze this circuit by first computing the output common-mode level. In the absence of oscillation, the circuit reduces to that shown in Fig. 8.30(b), where M_1 and M_2 share I_{DD} equally and are configured as diode-connected devices. Thus, the CM level is simply given by the gate-source voltage of a diode-connected transistor carrying a current of $I_{DD}/2$.[4] For example, for square-law devices,

$$V_{GS1,2} = \sqrt{\frac{I_{DD}}{\mu_n C_{ox}(W/L)}} + V_{TH}. \tag{8.66}$$

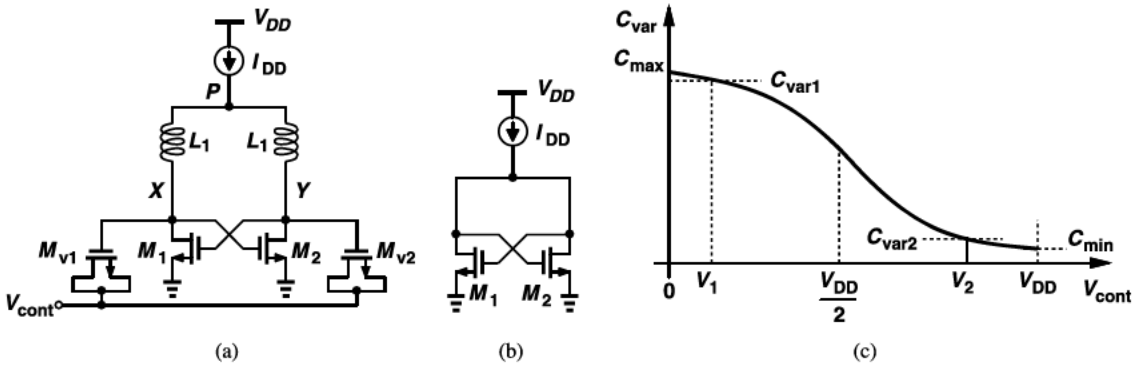

Figure 8.30 *(a) Top-biased VCO, (b) equivalent circuit for CM calculation, (c) varactor range used.*

We select the transistor dimensions such that the CM level is approximately equal to $V_{DD}/2$. Consequently, as V_{cont} varies from 0 to V_{DD}, the gate-source voltage of the varactors, $V_{GS,var}$, goes from $+V_{DD}/2$ to $-V_{DD}/2$, sweeping almost the entire capacitance range from C_{min} to C_{max} [Fig. 8.30(c)]. In practice, the circuit producing V_{cont} (the charge pump) can handle only the voltage range from V_1 to V_2, yielding a capacitance range from C_{var1} to C_{var2}.

The startup condition, oscillation frequency, and output swing of the oscillator shown in Fig. 8.30(a) are similar to those derived for the tail-biased circuit of Fig. 8.18(b). Also, L_1 and L_2 are realized as a single symmetric inductor so as to achieve a higher Q; the center tap of the inductor is tied to I_{DD}.

While providing a wider range than its tail-biased counterpart, the topology of Fig. 8.30(a) suffers from a higher phase noise. As studied in Section 8.7, this penalty arises primarily from the modulation of the output CM level (and hence the varactors) by the noise current of I_{DD}, as evidenced by Eq. (8.66). This effect does not occur in the tail-biased oscillator because the output CM level is "pinned" at V_{DD} by the low dc resistance of the inductors. The following example illustrates this difference.

4. With large-signal oscillation, the nonlinearity of M_1 and M_2 shifts the output CM level slightly, but we neglect this effect here.

Example 8.16

The tail or top bias current in the above oscillators is changed by ΔI. Determine the change in the voltage across the varactors.

Solution:

As shown in the tail-biased topology of Fig. 8.31(a), each inductor contains a small low-frequency resistance, r_s (typically no more than 10 Ω). If I_{SS} changes by ΔI, the output CM level changes by $\Delta V_{CM} = (\Delta I/2)r_s$, and so does the voltage across each varactor. In the top-biased circuit of Fig. 8.31(b), on the other hand, a change of ΔI flows through two diode-connected transistors, producing an output CM change of $\Delta V_{CM} = (\Delta I/2)(1/g_m)$. Since $1/g_m$ is typically in the range of a few hundred ohms, the top-biased topology suffers from a much higher varactor voltage modulation.

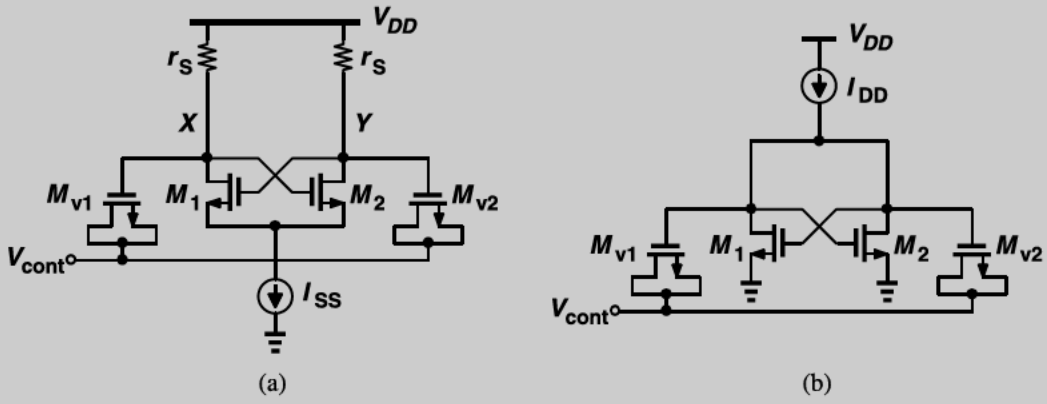

Figure 8.31 *Output CM dependence on bias current in (a) tail-biased and (b) top-biased VCOs.*

Example 8.17

What is the change in the oscillation frequency in the above example?

Solution:

Since a CM change at X and Y is indistinguishable from a change in V_{cont}, we have

$$\Delta\omega = K_{VCO}\Delta V_{CM} \tag{8.67}$$

$$= K_{VCO}\frac{\Delta I}{2}r_s \quad \text{or} \quad K_{VCO}\frac{\Delta I}{2}\frac{1}{g_m}. \tag{8.68}$$

In order to avoid varactor modulation due to the noise of the bias current source, we return to the tail-biased topology but employ *ac coupling* between the varactors and the core so as to allow positive and negative voltages across the varactors. Illustrated in Fig. 8.32(a),

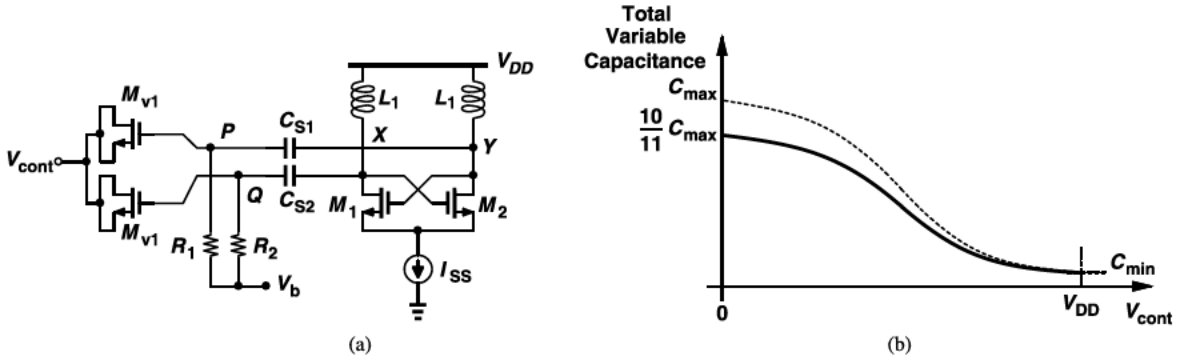

Figure 8.32 *(a) VCO using capacitor coupling to varactors, (b) reduction of tuning range as a result of finite C_{S1} and C_{S2}.*

the idea is to define the dc voltage at the gate of the varactors by V_b ($\approx V_{DD}/2$) rather than V_{DD}. Thus, in a manner similar to that shown in Fig. 8.30(c), the voltage across each varactor goes from $-V_{DD}/2$ to $+V_{DD}/2$ as V_{cont} varies from 0 to V_{DD}, maximizing the tuning range.

The principal drawback of the above circuit stems from the parasitics of the coupling capacitors. In Fig. 8.32(a), C_{S1} and C_{S2} must be *much greater* than the maximum capacitance of the varactors, C_{max}, so that the capacitance range presented by the varactors to the tanks does not shrink substantially. If $C_{S1} = C_{S2} = C_S$, then in Eq. (8.53), C_{var2} and C_{var1} must be placed in series with C_S, yielding

$$\Delta\omega_{os} \approx \frac{1}{\sqrt{L_1 C_1}} \cdot \frac{1}{2C_1} \cdot \frac{C_S^2(C_{var2} - C_{var1})}{(C_S + C_{var2})(C_S + C_{var1})}. \tag{8.69}$$

For example, if $C_S = 10C_{max}$, then the series combination yields a maximum capacitance of $(10C_{max} \cdot C_{max})/(11C_{max}) = (10/11)C_{max}$, i.e., about 10% less than C_{max}. Thus, as shown in Fig. 8.32(b), the capacitance range decreases by about 10%. Equivalently, the maximum-to-minimum capacitance ratio falls from C_{max}/C_{min} to $(10C_{max} + C_{min})/(11C_{min}) \approx (10/11)(C_{max}/C_{min})$.