7.5 VARACTORS

As described in Chapter 8, "varactors" are an essential component of LC VCOs. Varactors also occasionally serve to tune the resonance frequency of narrowband amplifiers.

A varactor is a voltage-dependent capacitor. Two attributes of varactors become critical in oscillator design: (1) the capacitance range, i.e., the ratio of the maximum and minimum capacitances that the varactor can provide, and (2) the quality factor of the varactor, which is limited by the parasitic series resistances within the structure. Interestingly, these two parameters trade with each other in some cases.

In older generations of RF ICs, varactors were realized as reverse-biased *pn* junctions. Illustrated in Fig. 7.66(a) is one example where the *p*-substrate forms the anode and the n^+ contact, the cathode. (The p^+ contact provides a low-resistance connection to

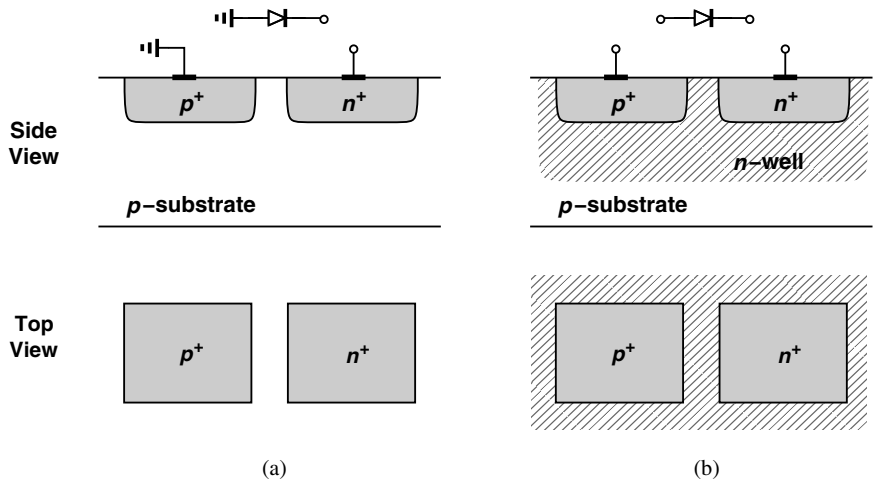

Figure 7.66 *PN junction varactor with (a) one terminal grounded, (b) both terminals floating.*

the substrate.) In this case, the anode is "hard-wired" to ground, limiting the design flexibility. A "floating" *pn* junction can be constructed as shown in Fig. 7.66(b), with an *n*-well isolating the diode from the substrate and acting as the cathode.

Let us examine the capacitance range and Q of *pn* junctions. At a reverse bias of V_D, the junction capacitance, C_j, is given by

$$C_j = \frac{C_{j0}}{\left(1 + \dfrac{V_D}{V_0}\right)^m}, \tag{7.109}$$

where C_{j0} is the capacitance at zero bias, V_0 the built-in potential, and m an exponent around 0.3 in integrated structures. We recognize the weak dependence of C_j upon V_D. Since $V_0 \approx 0.7$ to 0.8 V and since V_D is constrained to less than 1 V by today's supply voltages, the term $1 + V_D/V_0$ varies between approximately 1 and 2. Furthermore, an m of about 0.3 weakens this variation, resulting in a capacitance range, $C_{j,max}/C_{j,min}$, of roughly 1.23. In practice, we may allow the varactor to experience some forward bias (0.2 to 0.3 V), thus obtaining a somewhat larger range.

The Q of a *pn*-junction varactor is given by the total series resistance of the structure. In the floating diode of Fig. 7.66(b), this resistance is primarily due to the *n*-well and can be minimized by selecting minimum spacing between the n^+ and p^+ contacts. Moreover, as shown in Fig. 7.67, each p^+ region can be surrounded by an n^+ ring to lower the resistance in two dimensions.

Unlike inductors, transformers, and T-lines, varactors are quite difficult to simulate and model, especially for Q calculations. Consider the displacement current flow depicted in Fig. 7.68(a). Due to the two-dimensional nature of the flow, it is difficult to determine or compute the equivalent series resistance of the structure. This issue arises partly because the sheet resistance of the *n*-well is typically measured by the foundry for contacts having a spacing greater than the depth of the *n*-well [Fig. 7.68(b)]. Since the current path in this case is different from that in Fig. 7.68(a), the *n*-well sheet resistance cannot be directly applied

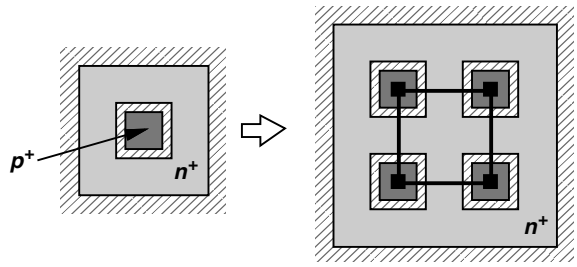

Figure 7.67 *Use of an n^+ ring to reduce varactor resistance.*

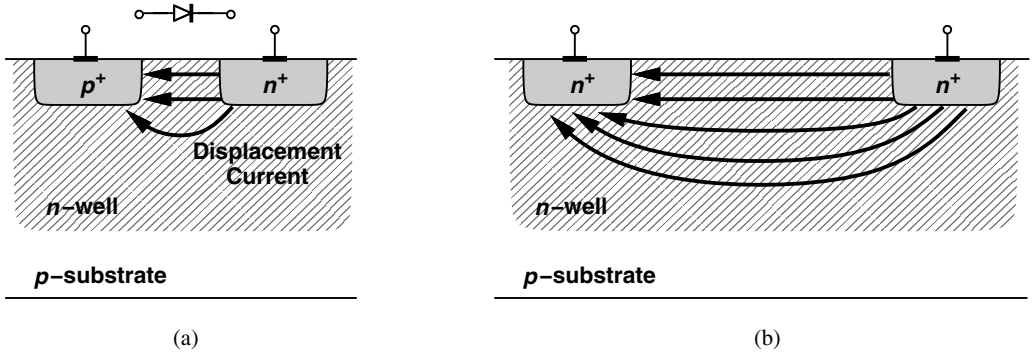

Figure 7.68 *Current distribution in a (a) varactor, (b) typical test structure.*

to the calculation of the varactor series resistance. For these reasons, the Q of varactors is usually obtained by measurement on fabricated structures.[15]

In modern RF IC design, MOS varactors have supplanted their *pn*-junction counterparts. A regular MOSFET exhibits a voltage-dependent gate capacitance (Fig. 7.69), but the nonmonotonic behavior limits the design flexibility. For example, a voltage-controlled oscillator (VCO) employing such a varactor would generate an output frequency that rises *and* falls as (the average) V_{GS} goes from negative to positive values. This nonmonotonic frequency tuning behavior becomes problematic in phase-locked loop design (Chapter 9).

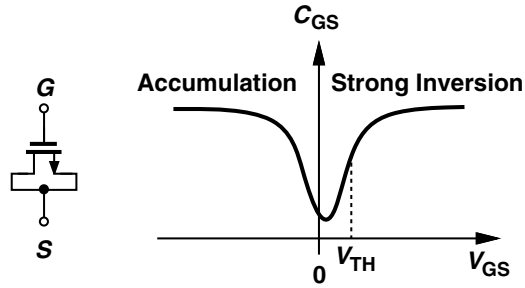

Figure 7.69 *Variation of gate capacitance with V_{GS}.*

15. Of course, semiconductor device simulators can be used here if the doping levels and the junction depths are known.

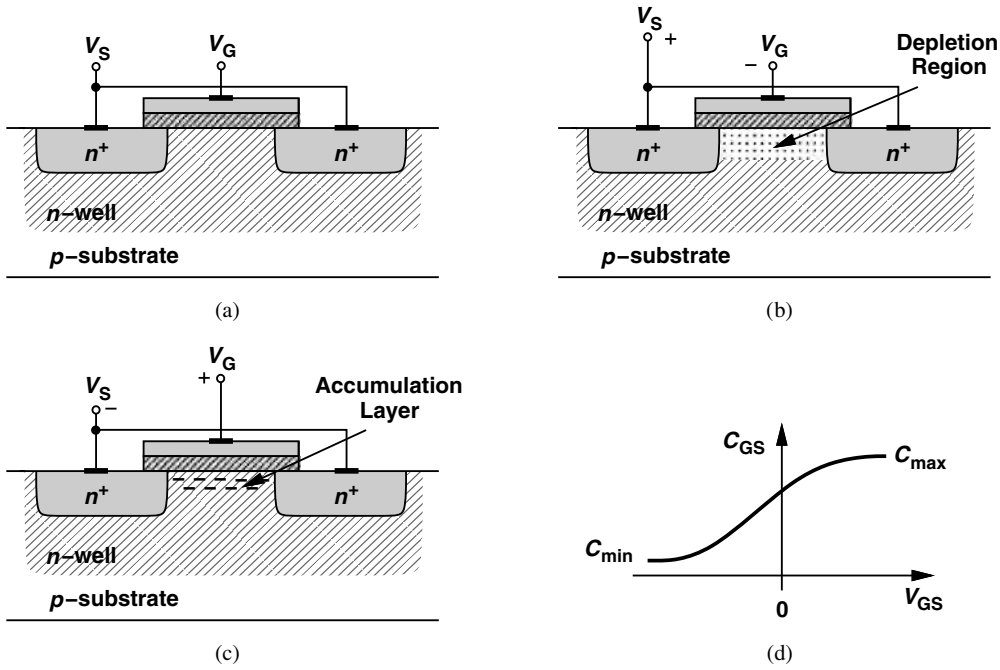

Figure 7.70 *(a) MOS varactor, (b) operation with negative gate-source voltage, (c) operation with positive gate-source voltage, (d) resulting C/V characteristic.*

A simple modification of the MOS device avoids the above issues. Called an "accumulation-mode MOS varactor" and shown in Fig. 7.70(a), this structure is obtained by placing an NMOS transistor inside an *n*-well. If $V_G < V_S$, then the electrons in the *n*-well are repelled from the silicon/oxide interface and a depletion region is formed [Fig. 7.70(b)]. Under this condition, the equivalent capacitance is given by the series combination of the oxide and depletion capacitances. As V_G exceeds V_S, the interface attracts electrons from the n^+ source/drain terminals, creating a channel [Fig. 7.70(c)]. The overall capacitance therefore rises to that of the oxide, behaving as shown in Fig. 7.70(d). (Since the material under the gate is *n*-type silicon, the concept of strong inversion does not apply here.)

The C/V characteristic of MOS varactors has scaled well with CMOS technology generations, approaching its saturated levels of C_{max} and C_{min} for $V_{GS} \approx \pm 0.5$ V in 65-nm devices. These varactors therefore operate with low supply voltages better than their *pn*-junction counterparts.

Another advantage of accumulation-mode MOS varactors is that, unlike *pn* junctions, they can tolerate both positive and negative voltages. In fact, the characteristic of Fig. 7.70(d) suggests that MOS varactors *should* operate with positive and negative biases so as to provide maximum tuning range. We pursue this point in VCO design in Chapter 8.

Circuit simulations must somehow incorporate the varactor C/V characteristic of Fig. 7.70(d). In practice, this characteristic is measured on fabricated devices and represented by a table of discrete values. Such a table, however, may introduce discontinuities in the *derivatives* of the characteristic, creating undesirable artifacts (e.g., a high noise floor) in simulations. It is therefore desirable to approximate the C/V plot by a well-behaved

function. The hyperbolic tangent proves useful here for both its saturating behavior and its continuous derivatives. Noting that $\tanh(\pm\infty) = \pm 1$, we approximate the characteristic of Fig. 7.70(d) by

$$C_{var}(V_{GS}) = \frac{C_{max} - C_{min}}{2} \tanh\left(a + \frac{V_{GS}}{V_0}\right) + \frac{C_{max} + C_{min}}{2}. \tag{7.110}$$

Here, a and V_0 allow fitting for the intercept and the slope, respectively, and C_{min} and C_{max} include the gate-drain and gate-source overlap capacitance.

The above varactor model translates to different characteristics in different circuit simulators! For example, HSPICE predicts a narrower oscillator tuning range than Cadence does. Simulation tools that analyze circuits in terms of voltages and currents (e.g., HSPICE) interpret the nonlinear capacitance equation correctly. On the other hand, programs that represent the behavior of capacitors by *charge equations* (e.g., Cadence's Spectre) require that the model be transformed to a Q/V relationship. To this end, we recall the general definition of capacitance from $dQ = C(V)dV$ and write

$$Q_{var} = \int C_{var} dV_{GS} \tag{7.111}$$

$$= \frac{C_{max} - C_{min}}{2} V_0 \ln\left[\cosh\left(a + \frac{V_{GS}}{V_0}\right)\right] + \frac{C_{max} + C_{min}}{2} V_{GS}. \tag{7.112}$$

In other words, the varactor is represented as a two-terminal device whose charge and voltage are related by Eq. (7.112). The simulation tool then computes the current flowing through the varactor as

$$I_{var} = \frac{dQ_{var}}{dt}. \tag{7.113}$$

The Q of MOS varactors is determined by the resistance between the source and drain terminals.[16] As shown in Fig. 7.71(a), this resistance and the capacitance are distributed from the source to the drain and can be approximated by the lumped model depicted in Fig. 7.71(b).

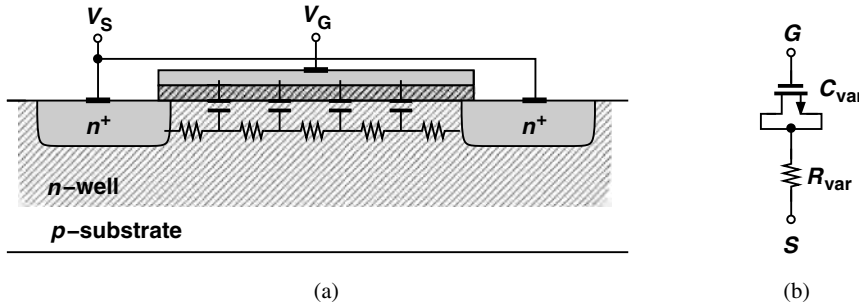

Figure 7.71 *(a) Effect of distributed resistance in a varactor, (b) lumped model.*

16. We assume that the gate resistance is minimized by proper layout.

Example 7.33

Determine the equivalent resistance and capacitance values in the lumped model of Fig. 7.71(b).

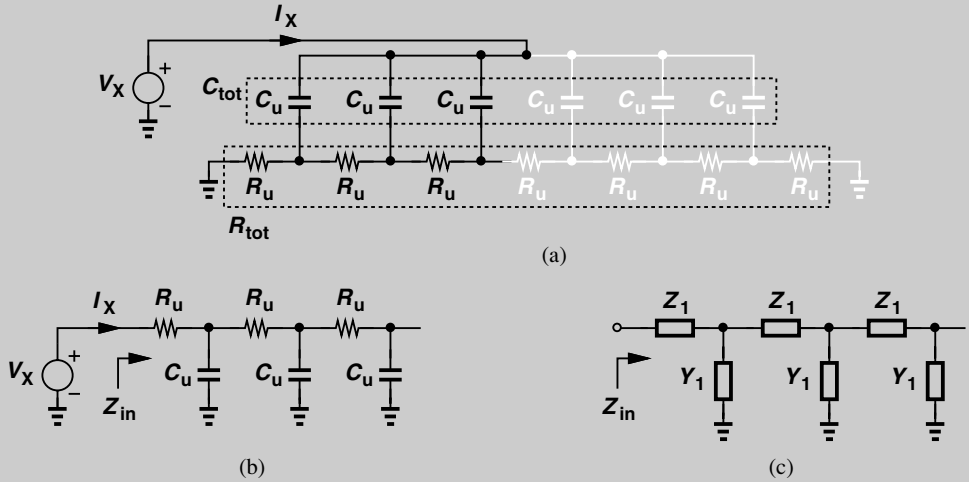

Figure 7.72 *(a) Distributed model of a varactor, (b) equivalent circuit for half of the structure, (c) canonical T-line structure.*

Solution:

Let us first consider only one-half of the structure as shown in Fig. 7.72(a). Here, the unit capacitances add up to the total distributed capacitance, C_{tot}, and the unit resistances to the total distributed resistance, R_{tot}. We turn the circuit upside down, arriving at the more familiar topology illustrated in Fig. 7.72(b). The circuit now resembles a transmission line consisting of series resistances and parallel capacitances. For the general T-line shown in Fig. 7.72(c), it can be proved that the input impedance, Z_{in}, is given by [18]

$$Z_{in} = \sqrt{\frac{Z_1}{Y_1}} \frac{1}{\tanh(\sqrt{Z_1 Y_1}\, d)}, \tag{7.114}$$

where Z_1 and Y_1 are specified for unit length and d is the length of the line. From Fig. 7.72(b), $Z_1 d = R_{tot}$ and $Y_1 d = C_{tot} s$; thus,

$$Z_{in} = \sqrt{\frac{R_{tot}}{C_{tot} s}} \frac{1}{\tanh(\sqrt{R_{tot} C_{tot} s/4})}. \tag{7.115}$$

At frequencies well below $1/(R_{tot}C_{tot}/4)$, the argument of tanh is much less than unity, allowing the approximation,

$$\tanh \epsilon \approx \epsilon - \frac{\epsilon^3}{3} \tag{7.116}$$

$$\approx \frac{\epsilon}{1 + \dfrac{\epsilon^2}{3}}. \tag{7.117}$$

Example 7.33 (*Continued*)

It follows that

$$Z_{in} \approx \frac{1}{C_{tot}s/2} + \frac{R_{tot}/2}{3}. \tag{7.118}$$

That is, the lumped model of half of the structure consists of its distributed capacitance in series with one-third of its distributed resistance. Accounting for the gray half in Fig. 7.72(b), we obtain

$$Z_{in,tot} \approx \frac{1}{C_{tot}s} + \frac{R_{tot}}{12}. \tag{7.119}$$

The principal difficulty in computing the Q of MOS varactors (placed inside an n-well) is that the resistance between the source and drain cannot be directly computed from the MOS transistor characteristics. As with pn junctions, the Q of MOS varactors is usually obtained from experimental measurements.

How does the Q of MOS varactors vary with the capacitance? In the characteristic of Fig. 7.70(d), as we begin from C_{min}, the capacitance is small and the resistance somewhat large (that of n-well). On the other hand, as we approach C_{max}, the capacitance rises and the resistance falls. Consequently, equation $Q = 1/(RC\omega)$ suggests that the Q may remain relatively constant. In practice, however, the Q drops as C_{GS} goes from C_{min} to C_{max} (Fig. 7.73), indicating that the relative rise in the capacitance is greater than the relative fall in the resistance.

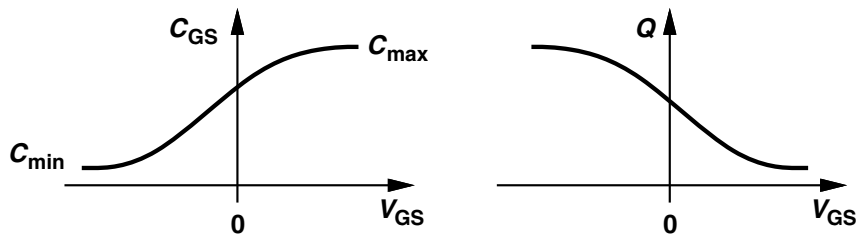

Figure 7.73 *Variation of varactor Q with capacitance.*

As explained in Chapter 8, it is desirable to maximize the Q of varactors for oscillator design. From our foregoing study of MOS varactors, we conclude that the device length (the distance between the source and drain) must be minimized. Unfortunately, for a minimum channel length, the overlap capacitance between the gate and source/drain terminals becomes a substantial fraction of the overall capacitance, limiting the capacitance range. As illustrated in Fig. 7.74, the overlap capacitance (which is relatively voltage-independent) shifts the C/V characteristic up, yielding a ratio of $(C_{max} + 2WC_{ov})/(C_{min} + 2WC_{ov})$, where C_{max} and C_{min} denote the "intrinsic" values, i.e., those without the overlap effect. For a minimum channel length, $2WC_{ov}$ may even be larger than C_{min}, thus reducing the capacitance ratio considerably.

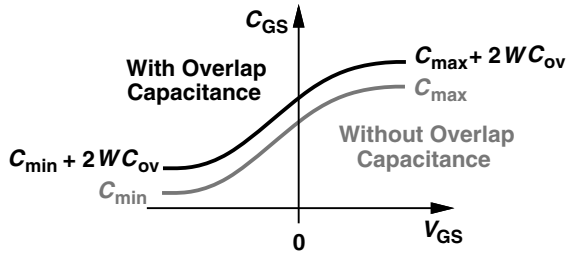

Figure 7.74 *Effect of overlap capacitance on varactor capacitance range.*

Example 7.34

A MOS varactor realized in 65-nm technology has an effective length of 50 nm and a C_{ov} of 0.09 fF/μm. If $C_{ox} = 17\,\text{fF}/\mu\text{m}^2$, determine the largest capacitance range that the varactor can provide.

Solution:

Assuming a width of 1 μm for the device, we have $2WC_{ov} = 0.18\,\text{fF}$ and a gate oxide capacitance of $17\,\text{fF}/\mu\text{m}^2 \times 1\,\mu\text{m} \times 50\,\text{nm} = 0.85\,\text{fF}$. Thus, the minimum capacitance is 0.18 fF (if the series combination of the oxide and depletion capacitances is neglected), and the maximum capacitance reaches $0.85\,\text{fF} + 0.18\,\text{fF} = 1.03\,\text{fF}$. The largest possible capacitance ratio is therefore equal to 5.72. In practice, the series combination of the oxide and depletion capacitances is comparable to $2WC_{ov}$, reducing this ratio to about 2.5.

In order to achieve a larger capacitance range, the length of MOS varactors can be increased. In the above example, if the effective channel length grows to 100 nm, then the capacitance ratio reaches $(1.7\,\text{fF} + 0.18\,\text{fF})/(0.18\,\text{fF}) = 10.4$. However, the larger source-drain resistance results in a lower Q. Since the maximum capacitance goes from 1.03 fF to 1.88 fF and since the channel resistance is doubled, the Q [$= 1/(RC\omega)$] falls by a factor of 3.65. In other words, an m-fold increase in the channel length translates to roughly an m^2-fold drop in the Q.

The trade-off between the capacitance range and Q of varactors ultimately leads to another between the tuning range and phase noise of LC VCOs. We study this issue in Chapter 8. At frequencies up to about 10 GHz, a channel length of twice the minimum may be chosen so as to widen the capacitance range while retaining a varactor Q much larger than the inductor Q.