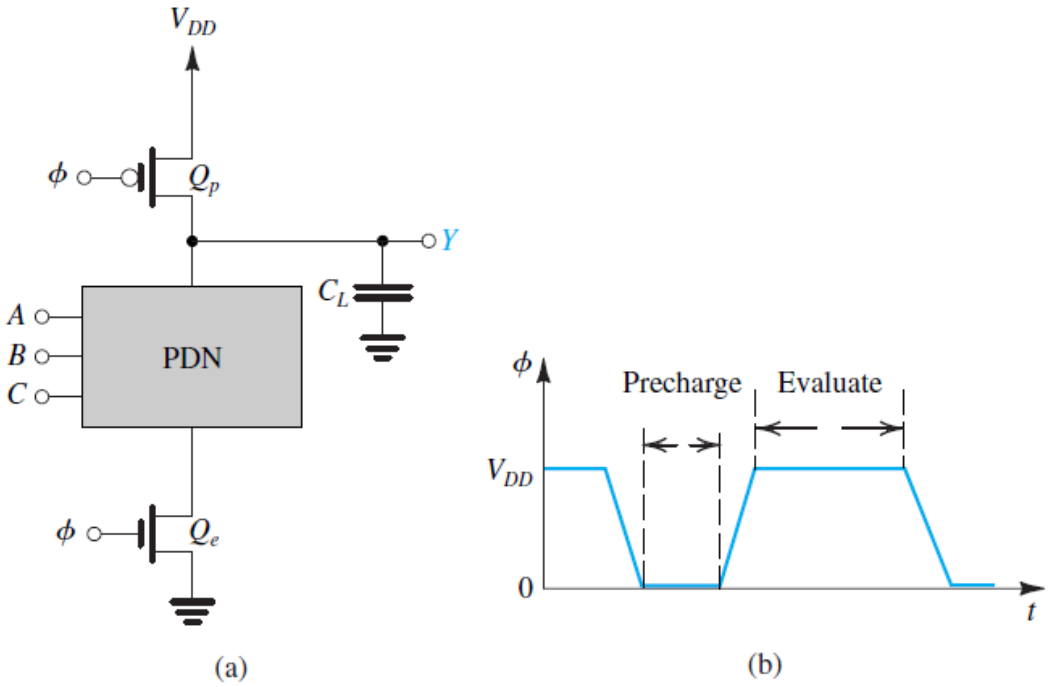
Dynamic Domino CMOS Logic

- One technique to help decrease power in MOS logic circuits is dynamic logic
- Dynamic logic uses different precharge and evaluation phases that are controlled by a system clock to eliminate the dc current path in single channel logic circuits
- Early MOS logic required multiphase clocks to accomplish this, but CMOS logic can be operated dynamically with a single clock

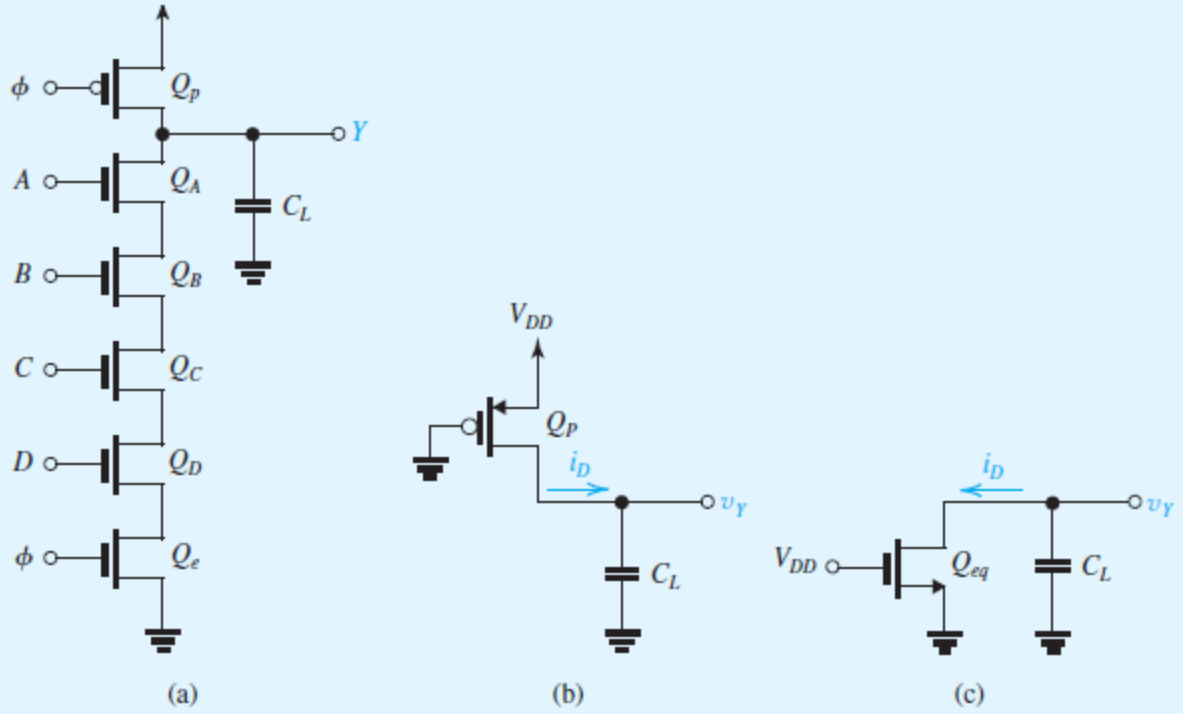
Dynamic CMOS Logic



Precharge phase (φ low) Qp ON
Evaluation phse (φ high) Qn ON

παράδειγμα

fabricated in a 0.18-µm CMOS technology for which $V_{DD} = 1.8$ V, $V_t = 0.5$ V, and $\mu_n C_{ox} = 4\mu_p C_{ox} = 300\ \mu A/V^2$. To keep C_L small, NMOS devices with $W/L = 0.27\ \mu m/0.18\ \mu m$ are used (including transistor Q_e). The PMOS precharge transistor Q_p has $W/L = 0.54\ \mu m/0.18\ \mu m$. The total capacitance C_L is found to be 20 fF.



παράδειγμα

$$i_D(0.1V_{DD}) = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{DD} - |V_{tp}|)^2$$

$$= \frac{1}{2} \times 75 \times \frac{0.54}{0.18}(1.8 - 0.5)^2$$

$$= 190.1\ \mu A$$

$$i_D(0.9V_{DD}) = \mu_p C_{ox}\left(\frac{W}{L}\right)_p \left[(V_{DD} - |V_{tp}|)(V_{DD} - 0.9V_{DD}) - \frac{1}{2}(V_{DD} - 0.9V_{DD})^2\right]$$

$$= 75 \times \frac{0.54}{0.18}\left[(1.8 - 0.5)(1.8 - 1.62) - \frac{1}{2}(1.8 - 1.62)^2\right]$$

$$= 49\ \mu A$$

$$t_r = \frac{C\Delta v_Y}{I_{av}}$$

$$= \frac{C(0.9V_{DD} - 0.1V_{DD})}{I_{av}}$$

$$t_r = \frac{20 \times 10^{-15} \times 0.8 \times 1.8}{119.6 \times 10^{-6}} = 0.19\ \text{ns}$$

παράδειγμα

A=B=C=D=1 (evaluation)

$$i_D(V_{DD}) = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)_{eq}(V_{DD} - V_t)^2$$

$$= \frac{1}{2} \times 300 \times 0.3(1.8 - 0.5)^2$$

$$= 76.1\ \mu A$$

At $v_Y = V_{DD}/2$, Q_{eq} will be operating in the triode region; thus,

$$i_D(V_{DD}/2) = (\mu_n C_{ox})\left(\frac{W}{L}\right)_{eq}\left[(V_{DD} - V_t)\frac{V_{DD}}{2} - \frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2\right]$$

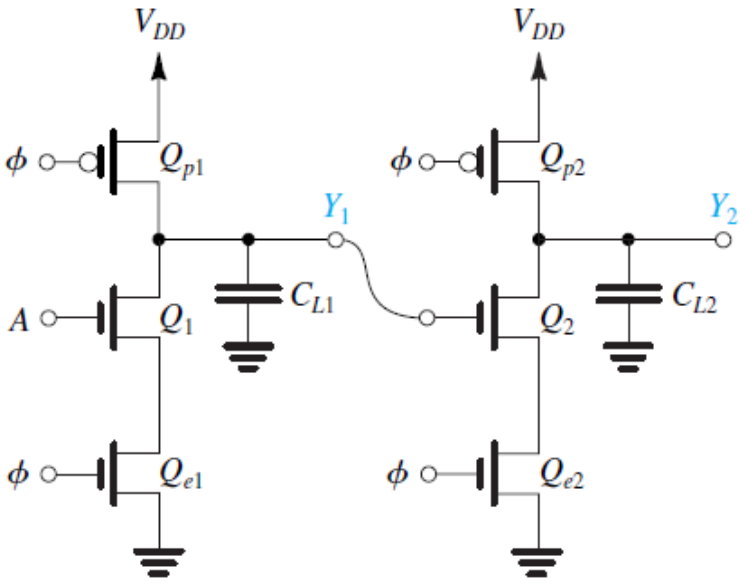
$$= 300 \times 0.3\left[(1.8 - 0.5)\left(\frac{1.8}{2}\right) - \frac{1}{2}\left(\frac{1.8}{2}\right)^2\right]$$

$$= 68.9\ \mu A$$

$$t_{PHL} = \frac{C(V_{DD} - V_{DD}/2)}{I_{av}}$$

$$= \frac{20 \times 10^{-15}(1.8 - 0.9)}{72.5 \times 10^{-6}} = 0.25\ ns$$

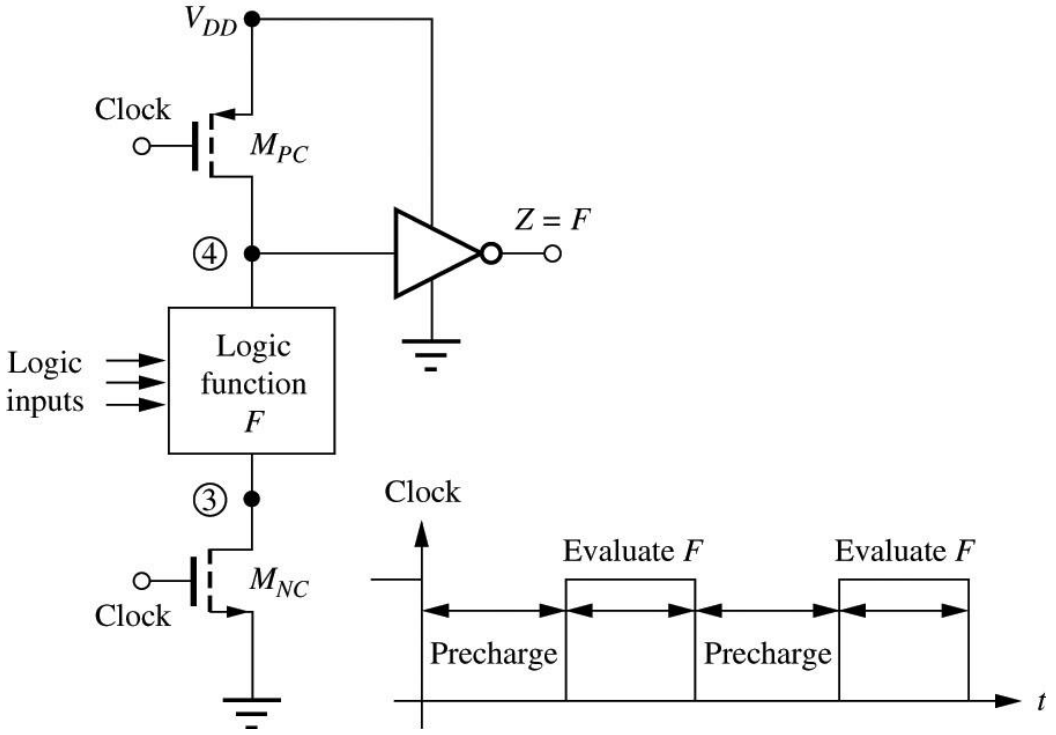
Cascading Dynamic Logic gates



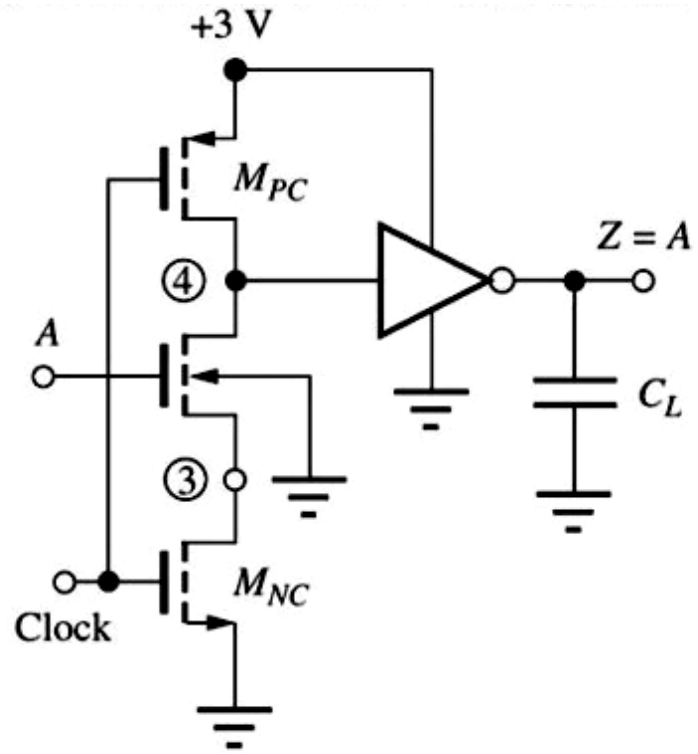
With A high, at evaluation phase *Q1* turns on discharging C_{L1} and **simultaneously** Q2 turns on discharging C_{L2} → ανεπιθύμητο διότι V_{Y2} πρέπει να είναι V_{DD}

Dynamic Domino CMOS Logic

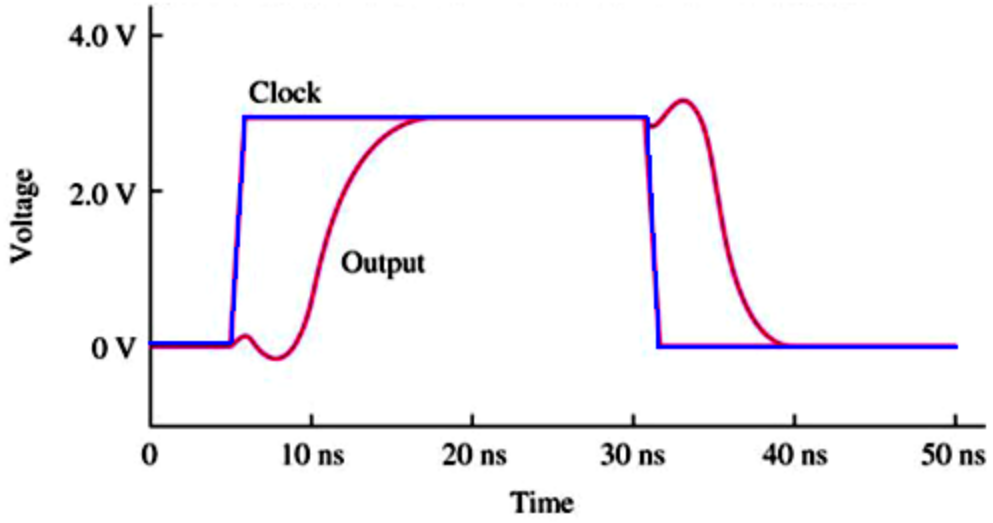
- The figure demonstrates the basic concept of domino CMOS logic operation



Simple Dynamic Domino Logic Circuit

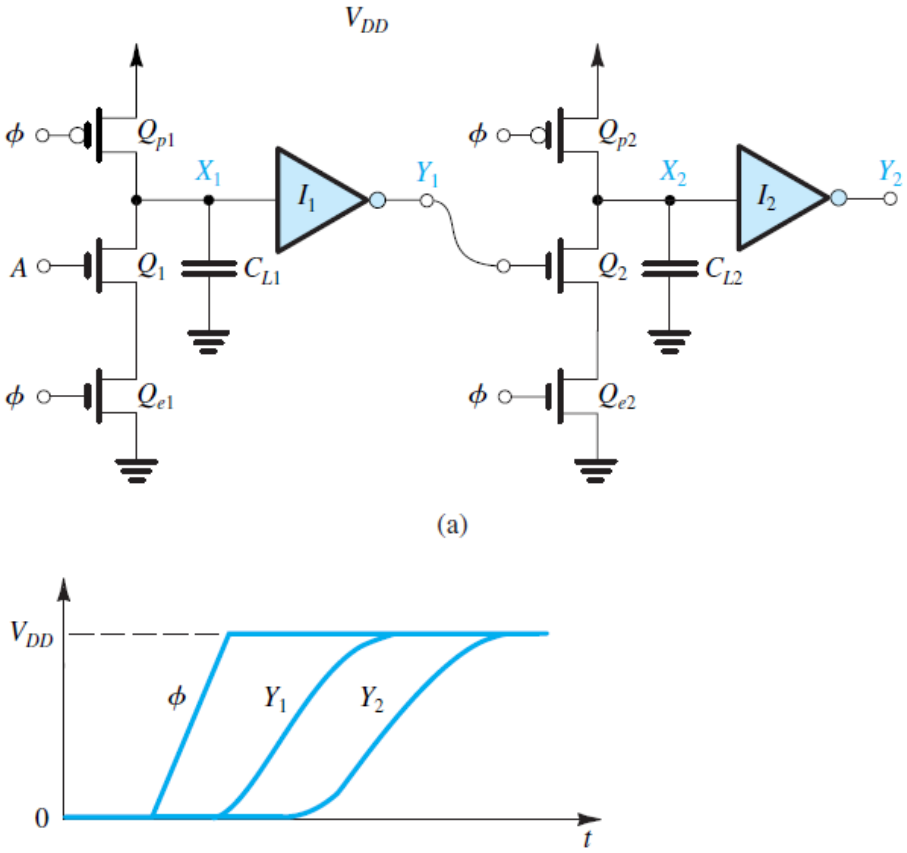


(a)



(b)

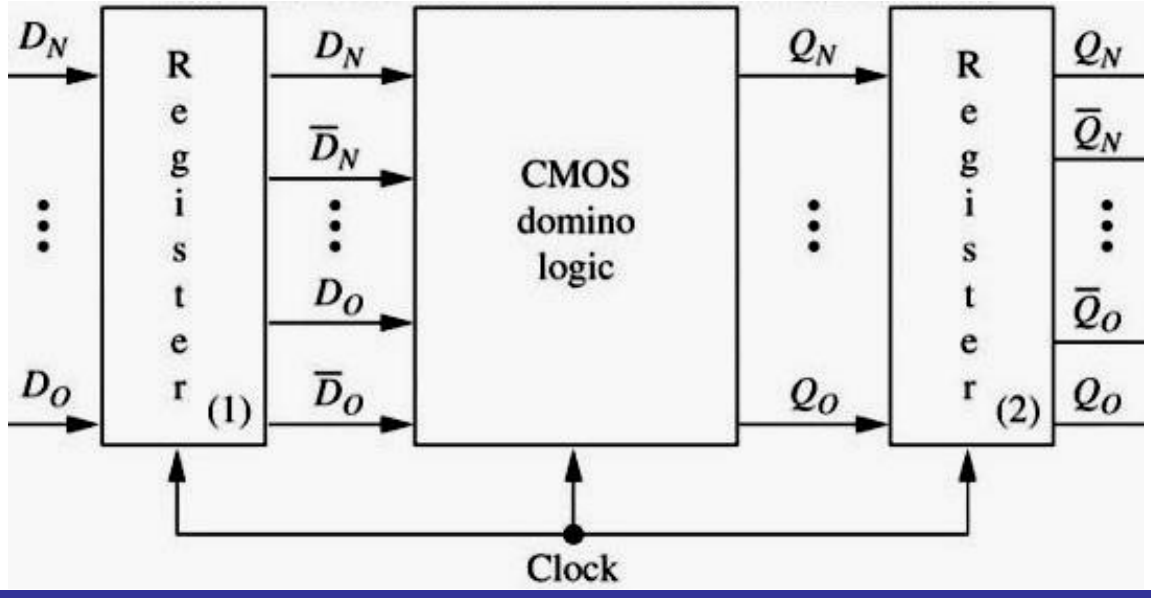
Domino CMOS Logic gates in cascade



Επειδή η έξοδος της πύλης Domino είναι low στην αρχή του evaluation, δεν γίνεται πρόωρη εκφόρτιση του C_{L2} στην επόμενη βαθμίδα

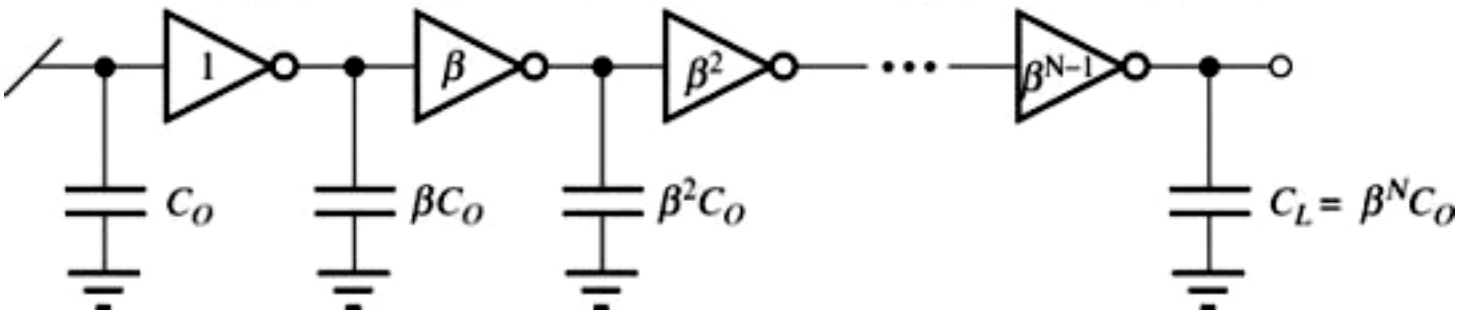
Dynamic Domino CMOS Logic

- It should be noted that domino CMOS circuits only produce true logic outputs, but this problem can be overcome by using registers that have both true and complemented outputs to complete the function shown by the following



Cascade Buffers

- In some circuits, the logic must be able to drive large capacitances (10 to 50 pF)
- By cascading a number of increasingly larger inverters, it is possible to drive the loads



Cascade Buffers

- The taper factor β determines the increase of the cascaded inverter's size in manner shown of the previous image.

$$\beta^N = \frac{C_L}{C_o}$$

where C_o is the unit inverter's load capacitance

- The delay of the cascaded buffer is given by the following:

$$\tau_B = N\left(\frac{C_L}{C_o}\right)^{1/N} \tau_o$$

where τ_o is the unit inverter's propagation delay

Optimum Design of Cascaded Stages

- The following expressions can aid in the design of an optimum cascaded buffer

$$N_{opt} = \ln\left(\frac{C_L}{C_o}\right)$$

$$\beta_{opt} = \left(\frac{C_L}{C_o}\right)^{\frac{1}{\ln\left(\frac{C_L}{C_o}\right)}} = \varepsilon$$

$$\tau_{Bopt} = \ln\left(\frac{C_L}{C_o}\right)\varepsilon\tau_o$$

παράδειγμα

$C_L = 50$ pF; technology has $C_o = 50$ fF.

Analysis: The optimum value of N is $N_{\text{opt}} = \ln C_L/C_o = \ln(1000) = 6.91$, and the optimum delay is $\tau_{B\text{opt}} = 6.91 \times (2.72) \times t_o = 18.8t_o$. N must be an integer, but either $N = 6$ or $N = 7$

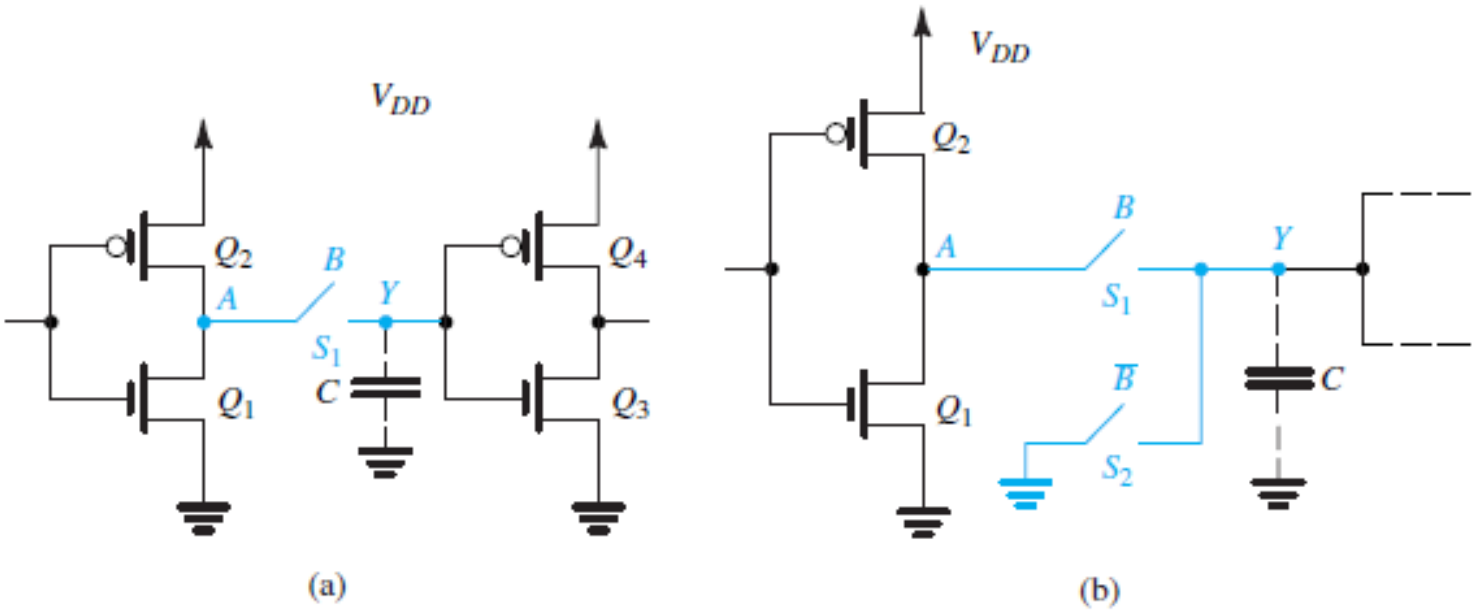
$$N = 6: \quad \tau_B = 6(1000^{1/6})\tau_o = 19.0\tau_o$$
$$N = 7: \quad \tau_B = 7(1000^{1/7})\tau_o = 18.8\tau_o$$

$$\beta = \left(\frac{C_L}{C_o}\right)^{1/N} = \left(\frac{50\text{ pF}}{50\text{ fF}}\right)^{1/6} = (1000)^{1/6} = \sqrt{10} = 3.16$$

$$\tau_o \cong \frac{2.4C}{K_n(V_{DD} - V_{TN})} = \frac{2.4(50\text{ fF})}{2(100\ \mu\text{A/V}^2)(3.3 - 0.75)} = 0.24\text{ ns}$$

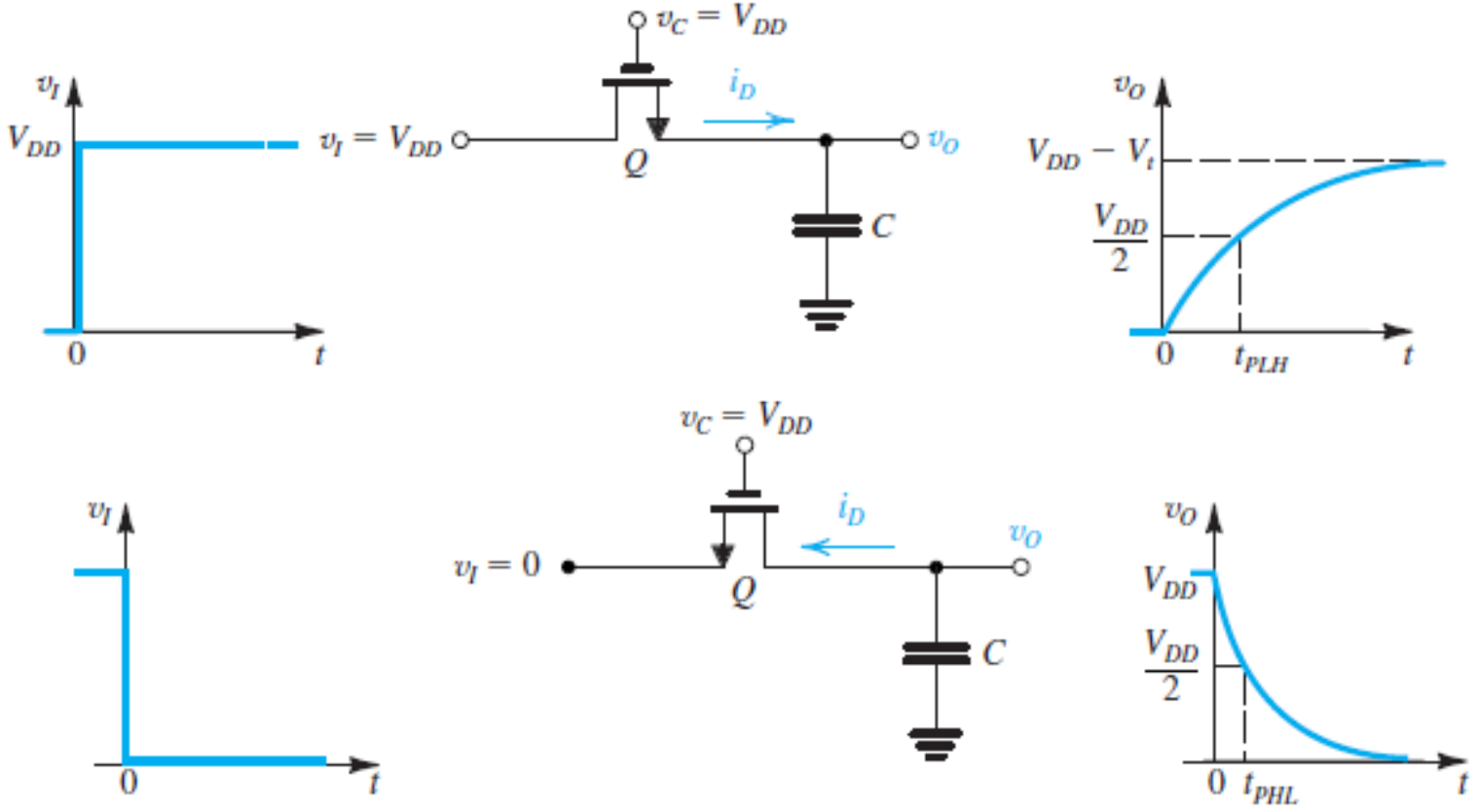
and the estimated buffer delay is $\tau_B = 4.5$ ns.

Pass Transistor Logic (PTL)



(a) Δεν υπάρχει Low resistance path
(b) Η διάταξη έχει Low resistance path

Pass Transistor Logic (PTL)- II



Παράδειγμα (I)

$\mu_n C_{ox} = 50\ \mu A/V^2,\ \mu_p C_{ox} = 20\ \mu A/V^2,\ |V_{t0}| = 1\ V,\ \gamma = 0.5\ V^{1/2},\ 2\phi_f = 0.6\ V,$

(W/L)n=2/1 , (W/L)p =5/1

$$V_{OH} = V_{DD} - V_t$$

where V_t is the value of the threshold voltage at a source–body reverse bias equal to V_{OH}. Using Eq. (14.21), we have

$$V_t = V_{t0} + \gamma\left(\sqrt{V_{OH} + 2\phi_f} - \sqrt{2\phi_f}\right)$$
$$= V_{t0} + \gamma\left(\sqrt{V_{DD} - V_t + 2\phi_f} - \sqrt{2\phi_f}\right)$$

$V_t = 1.6\ V$

$V_{OH} = 3.4\ V$

Παράδειγμα (II)

$$i_D(0) = \frac{1}{2} \times 50 \times \frac{4}{2} \times (5-1)^2 = 800\ \mu\text{A}$$

$$V_t\,(\text{at } v_O = 2.5\ \text{V}) = 1 + 0.5(\sqrt{2.5+0.6} - \sqrt{0.6}) = 1.49\ \text{V}$$

$$i_D(t_{PLH}) = \frac{1}{2} \times 50 \times \frac{4}{2}(5-2.5-1.49)^2 = 50\ \mu\text{A}$$

$$i_D\big|_{\text{av}} = \frac{800+50}{2} = 425\ \mu\text{A}$$

$$t_{PLH} = \frac{C(V_{DD}/2)}{i_D\big|_{\text{av}}}$$

$$= \frac{50 \times 10^{-15} \times 2.5}{425 \times 10^{-6}} = 0.29\ \text{ns}$$

Παράδειγμα (III)

$$i_D(0) = \frac{1}{2} \times 50 \times \frac{4}{2}(5-1)^2 = 800\ \mu\text{A}$$

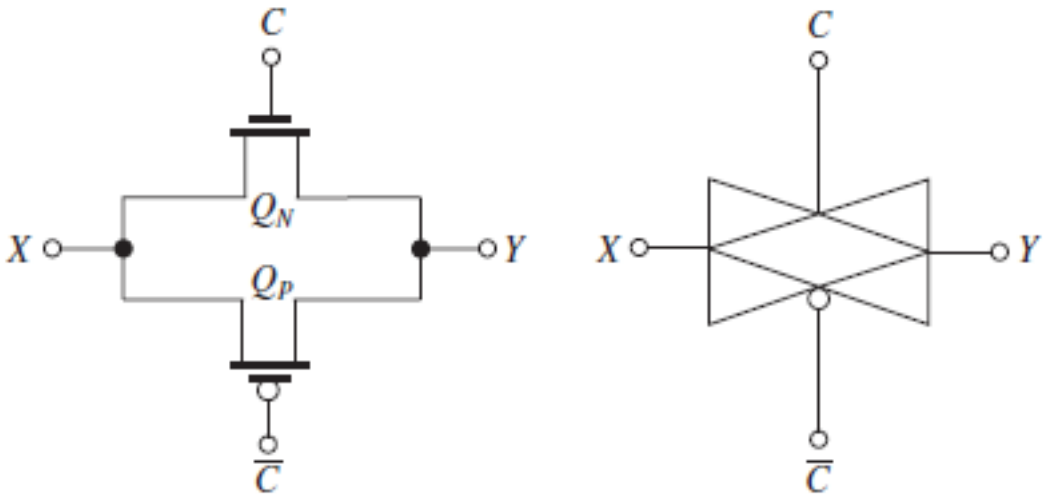
$$i_D(t_{PHL}) = 50 \times \frac{4}{2}\left[(5-1) \times 2.5 - \frac{1}{2} \times 2.5^2\right]$$
$$= 690\ \mu\text{A}$$

$$i_D\big|_{av} = \frac{1}{2}(800 + 690) = 740\ \mu\text{A}$$

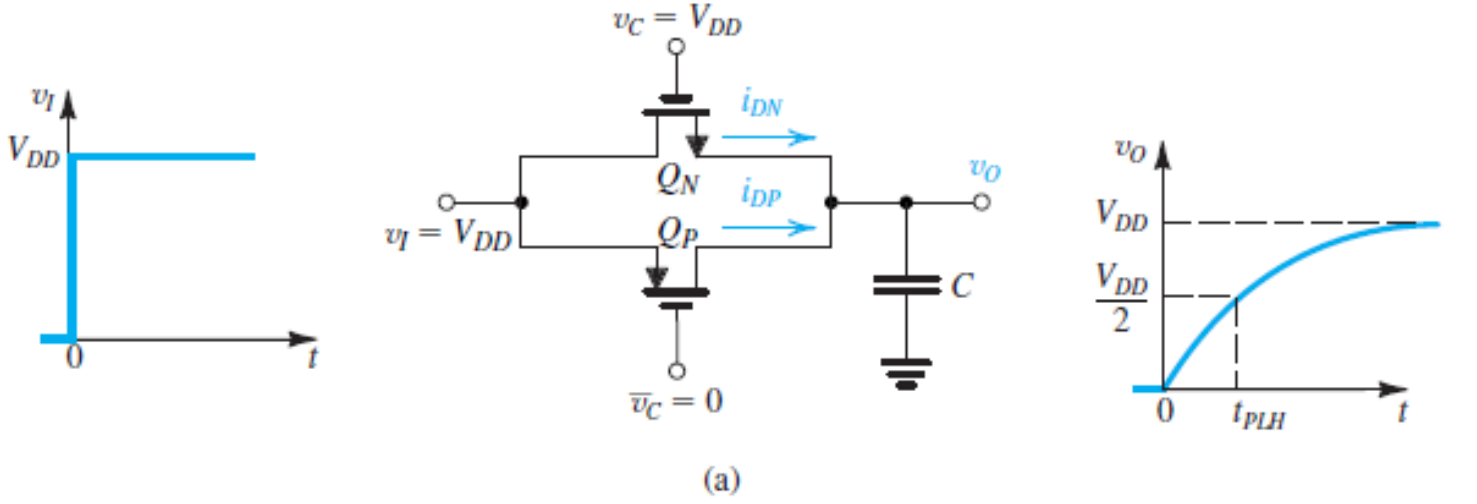
$$t_{PHL} = \frac{50 \times 10^{-15} \times 2.5}{740 \times 10^{-6}} = 0.17\ \text{ns}$$

$$t_P = \frac{1}{2}(t_{PLH} + t_{PHL}) = \frac{1}{2}(0.29 + 0.17) = 0.23\ \text{ns}$$

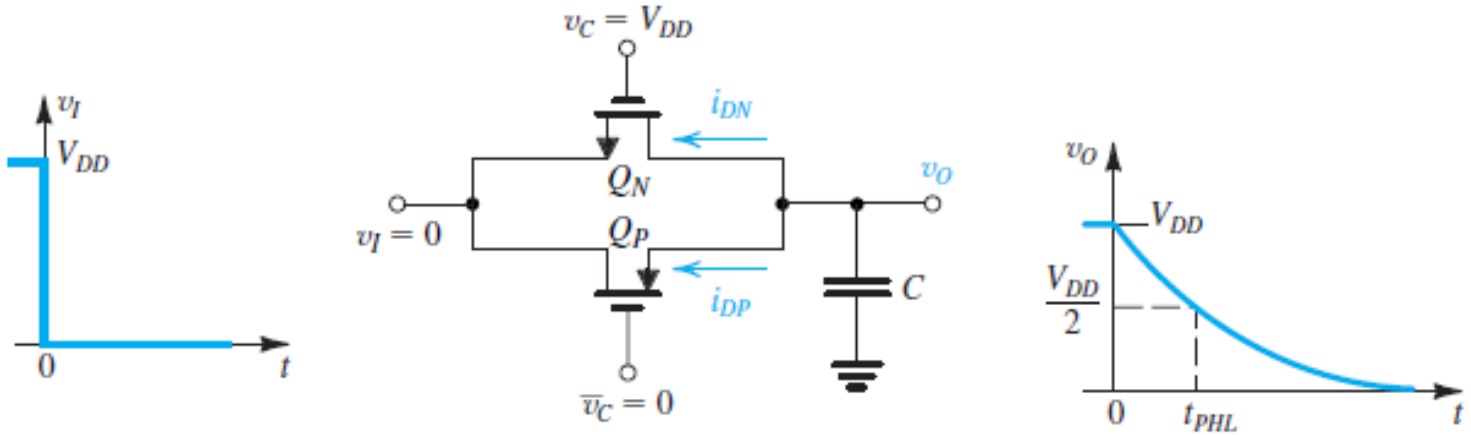
Υλοποίηση Διακοπτών με CMOS Transmission Gate



Λειτουργία Transmission gate (I)



(a)



(b)

Λειτουργία Transmission gate (II)

Κύκλωμα (α)

$$i_{DN} = \frac{1}{2}k_n(V_{DD} - v_O - V_{tn})^2$$

$$V_{tn} = V_{t0} + \gamma(\sqrt{v_O + 2\phi_f} - \sqrt{2\phi_f})$$

Q_N will conduct a diminishing current that reduces to zero at $v_O = V_{DD} - V_{tn}$.

Το ***Qp*** **όμως θα συνεχίσει να άγει** μέχρι να φορτιστεί πλήρως ο πυκνωτής και $Vo=V_H=V_{DD.}$
Το PMOS δίνει στην πύλη ένα"καλό 1"

Ισοδύναμη αντίσταση μιας Transmission gate

$$i_{DN} = \frac{1}{2}k_n(V_{DD} - V_{tn} - v_O)^2 \quad \text{for} \quad v_O \le V_{DD} - V_{tn}$$

$$i_{DN} = 0 \quad \text{for} \quad v_O \ge V_{DD} - V_{tn}$$

$$R_{Neq} = \frac{V_{DD} - v_O}{\frac{1}{2}k_n(V_{DD} - V_{tn} - v_O)^2} \quad \text{for} \quad v_O \le V_{DD} - V_{tn}$$

$$R_{Neq} = \infty \quad \text{for} \quad v_O \ge V_{DD} - V_{tn}$$

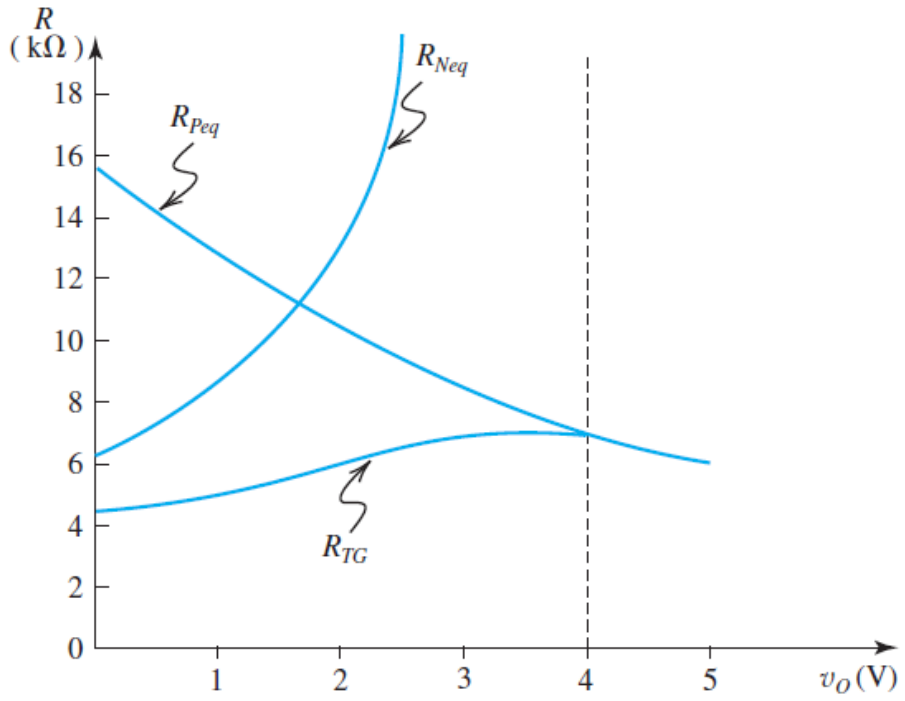
$$i_{DP} = \frac{1}{2}k_p(V_{DD} - |V_{tp}|)^2 \quad \text{for} \quad v_O \le |V_{tp}|$$

$$i_{DP} = k_p\left[(V_{DD} - |V_{tp}|)(V_{DD} - v_O) - \frac{1}{2}(V_{DD} - v_O)^2\right] \quad \text{for} \quad v_O \ge |V_{tp}|$$

$$R_{Peq} = \frac{V_{DD} - v_O}{\frac{1}{2}k_p(V_{DD} - |V_{tp}|)^2} \quad \text{for} \quad v_O \le |V_{tp}|$$

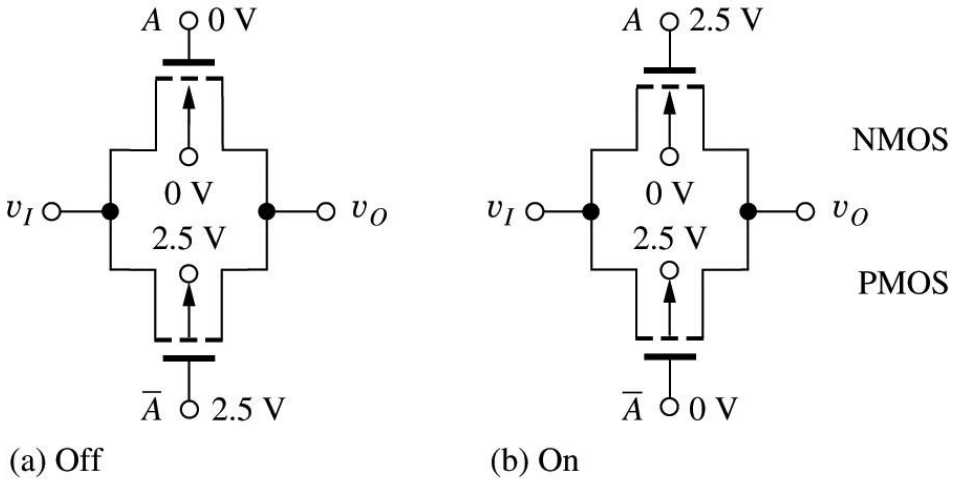
$$R_{Peq} = \frac{1}{k_p\left[V_{DD} - |V_{tp}| - \frac{1}{2}(V_{DD} - v_O)\right]} \quad \text{for} \quad v_O \ge |V_{tp}|$$

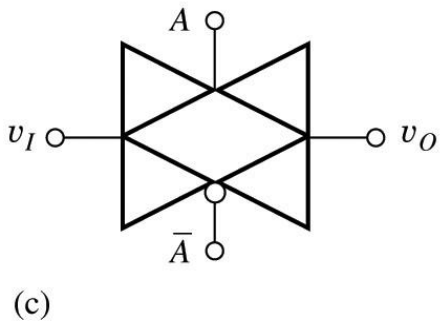
Ισοδύναμη αντίσταση μιας Transmission gate



$$R_{TG} = R_{Neq} \| R_{Peq}$$

The CMOS Transmission Gate





- The CMOS transmission gate (T-gate) is a useful circuits for both analog and digital applications
- It acts as a switch that can operate up to V_{DD} and down to V_{SS}

The CMOS Transmission Gate

- The main consideration that needs to be considered is the equivalent on-resistance which is given by the following expression:

$$R_{EQ} = \frac{R_{onp} R_{onn}}{R_{onp} + R_{onn}}$$