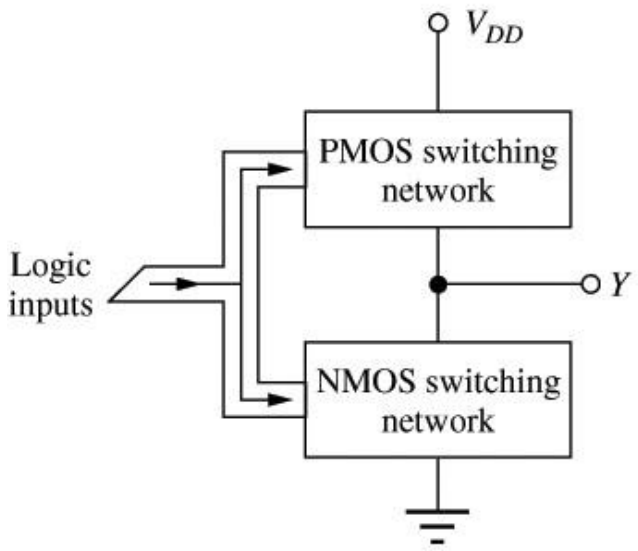
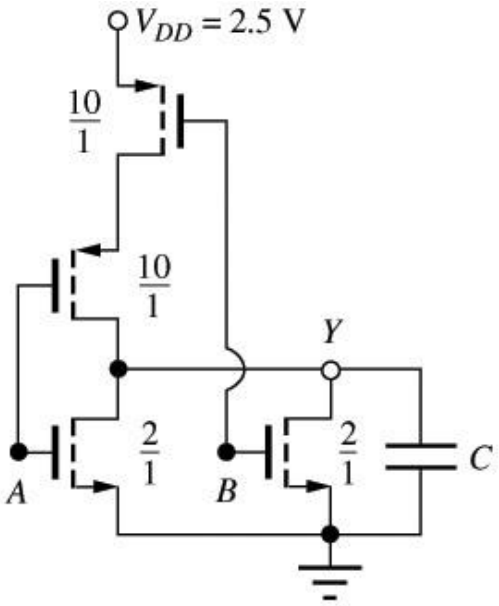
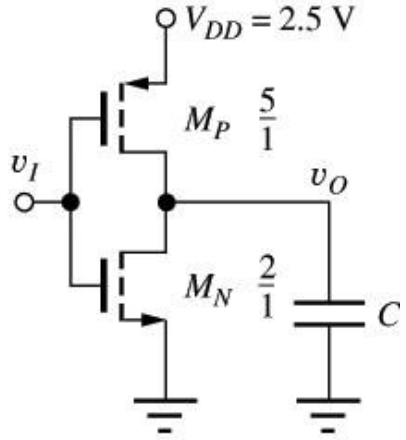
CMOS NOR Gate



Basic CMOS logic gate structure



CMOS NOR gate implementation



Reference Inverter

CMOS NOR Gate Transistor Sizing

- When sizing the transistors, we attempt to keep the delay times the same as the reference inverter
- To accomplish this, the on-resistance in the PMOS and NMOS branches of the NOR gate must be the same as the reference inverter
- For a two-input NOR gate, the $(W/L)_p$ must be made twice as large

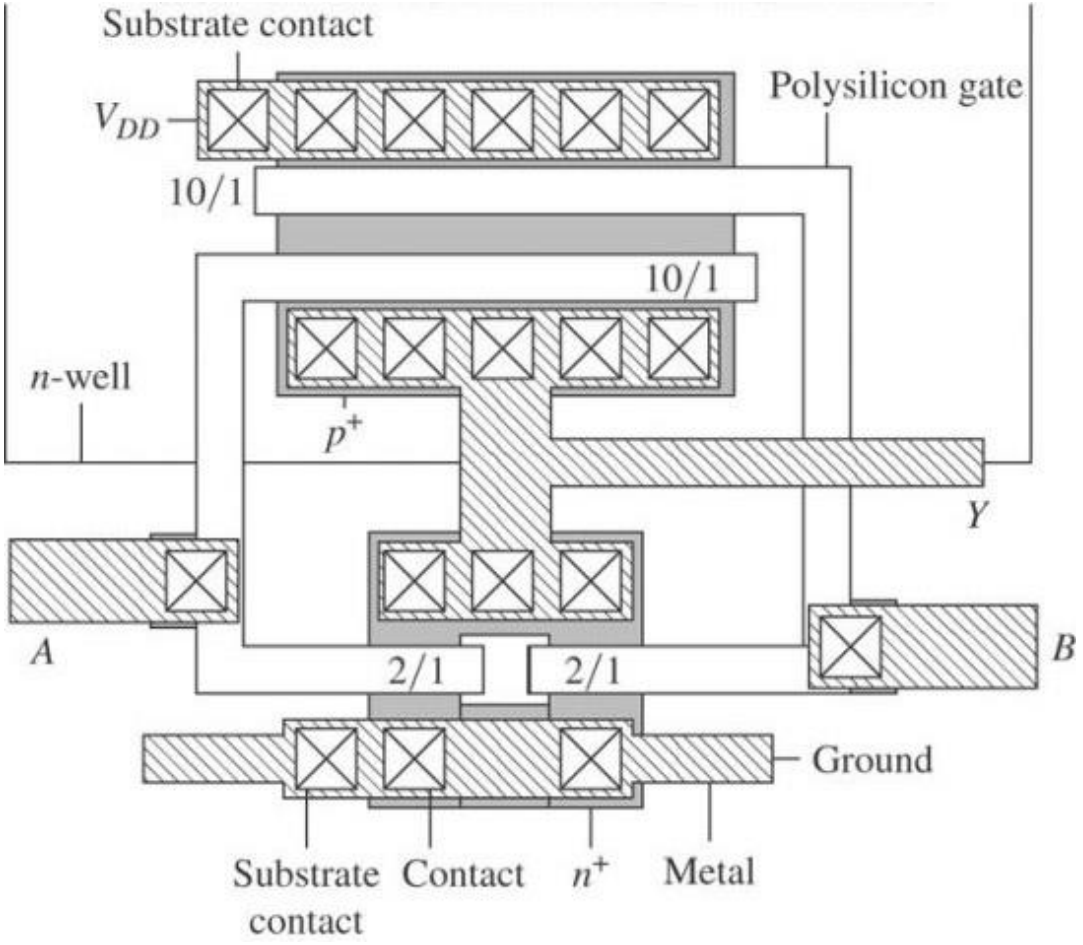
CMOS NOR Gate Body Effect

- Since the bottom PMOS body contact is not connected to its source, its threshold voltage changes as V_{SB} changes during switching

- Once $v_O = V_H$ is reached, the bottom PMOS is not affected by body effect, thus the total on-resistance of the PMOS branch is the same

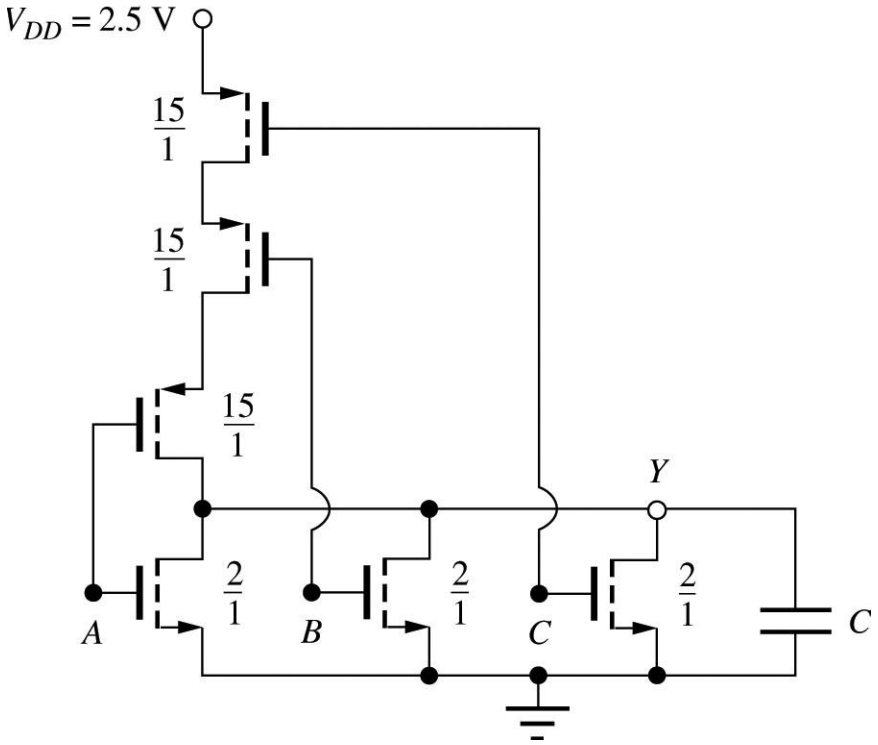
- However, the rise time is slowed down slightly due to $|V_{TP}|$ being a function of time

Two-Input NOR Gate Layout

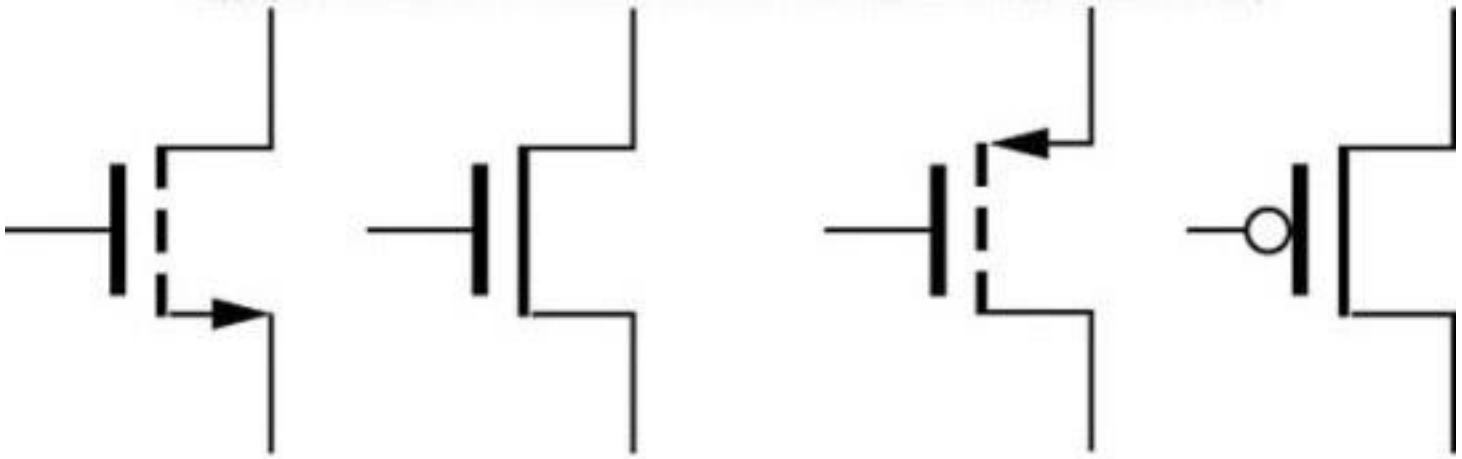


Three-Input NOR Gate Layout

- It is possible to extend this same design technique to create multiple input NOR gates

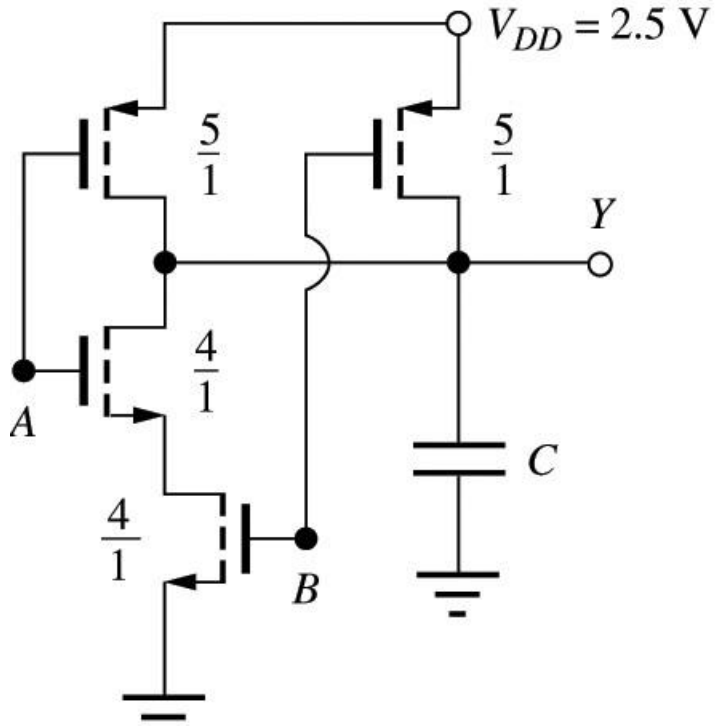


Shorthand Notation for NMOS and PMOS Transistors

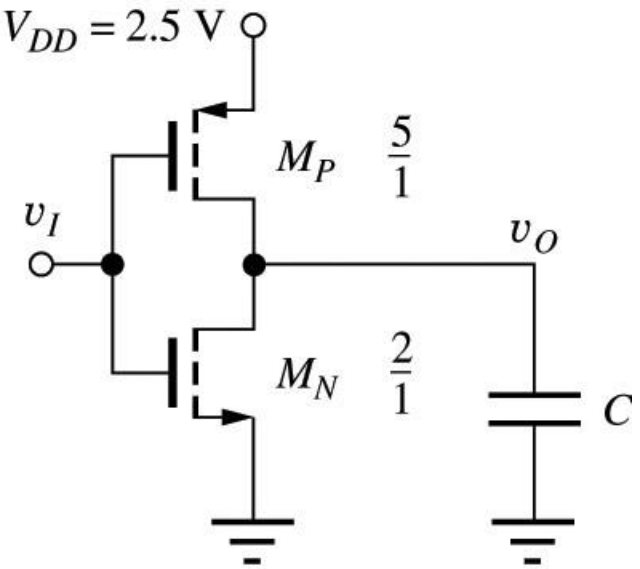


NMOS transistors PMOS transistors

CMOS NAND Gates



CMOS NAND gate implementation



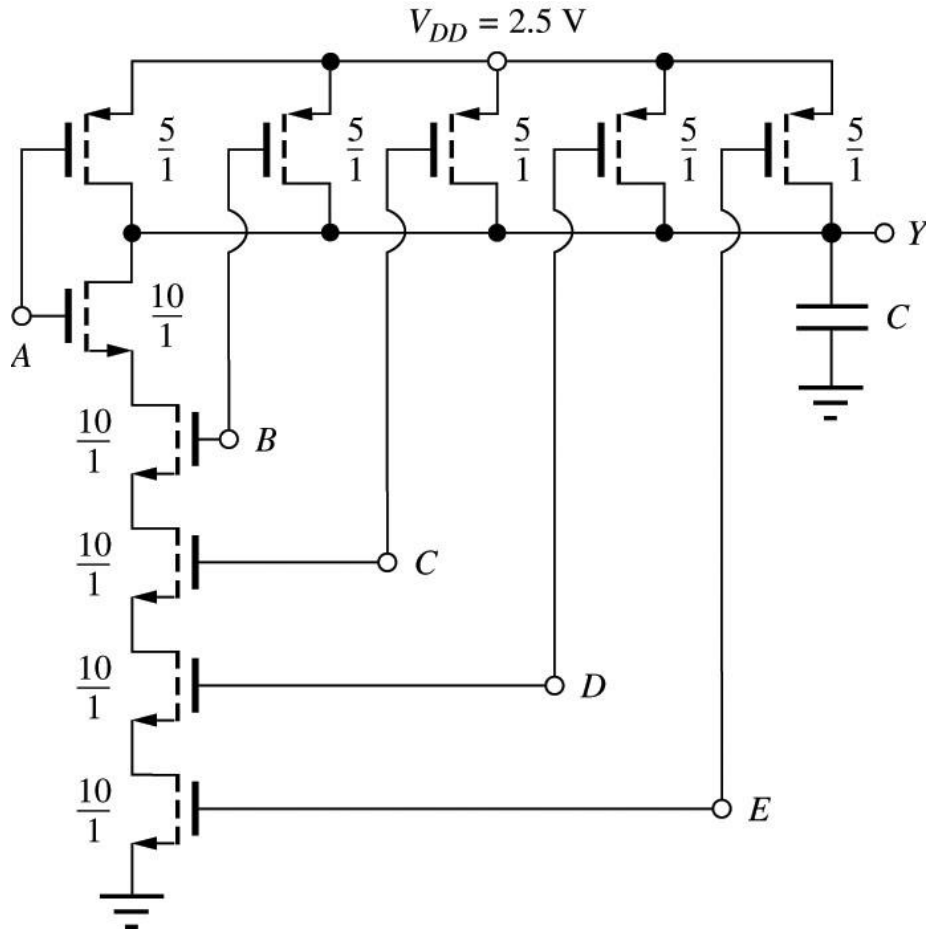
Reference Inverter

CMOS NAND Gate Transistor Sizing

- The same rules apply for sizing the NAND gate devices as for the NOR gate, except now the NMOS transistors are in series

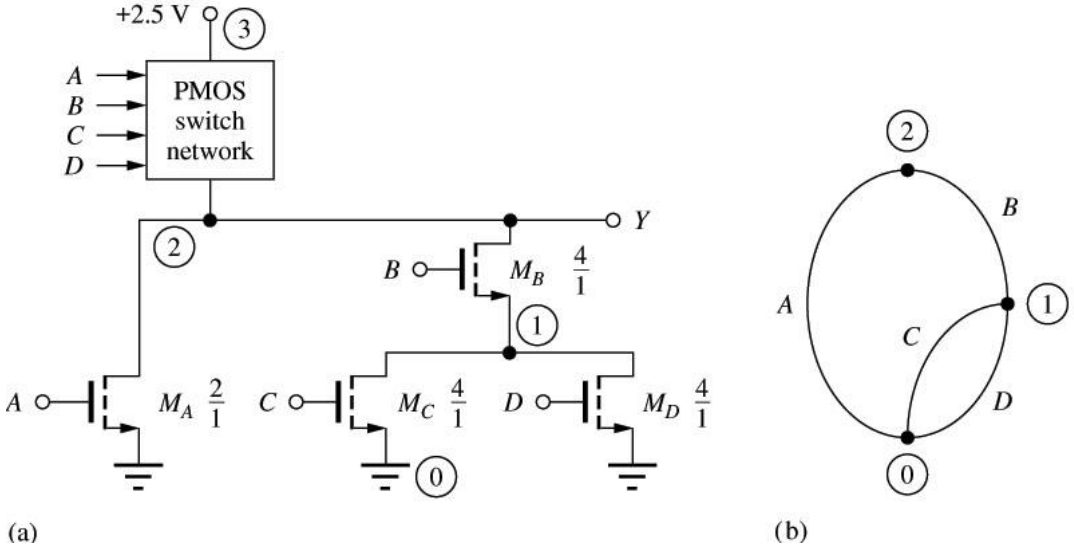
- $(W/L)_N$ will be twice the size of that of the reference inverter

Multi-Input CMOS NAND Gates



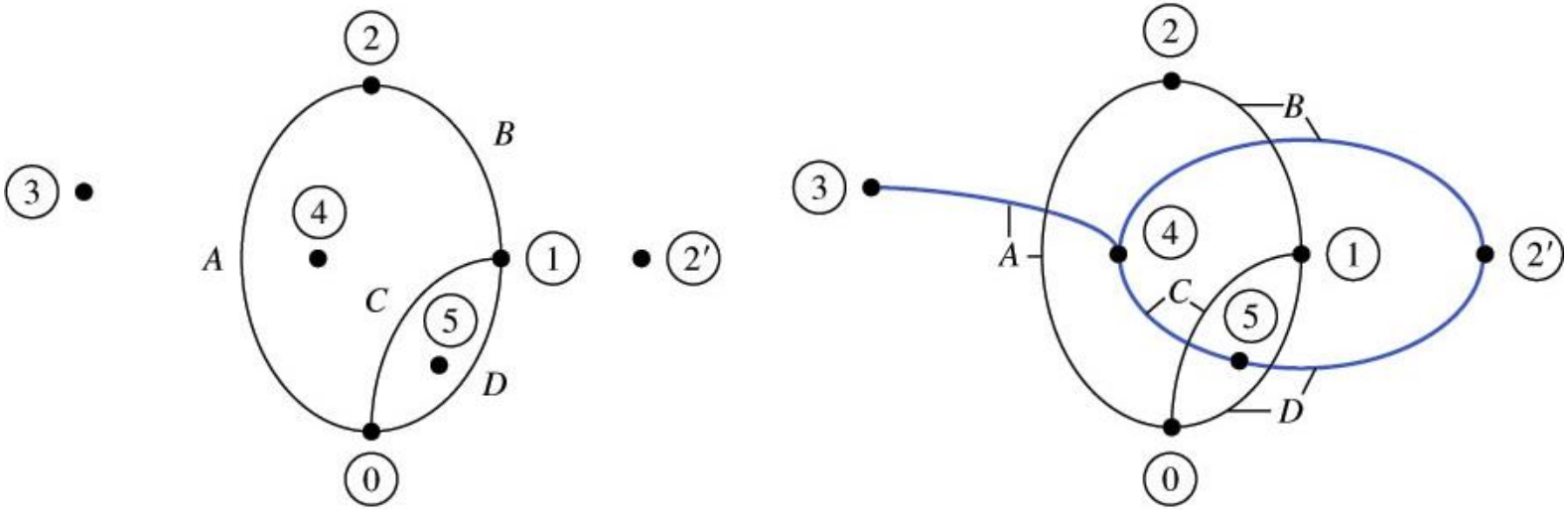
Complex CMOS Logic Gate Design Example – Euler path

- Design a CMOS logic gate for $(W/L)_{p,ref} = 5/1$ and for $(W/L)_{n,ref} = 2/1$ that yields the function: $Y = A + BC + BD$
- By inspection (knowing $\overline{Y}$), the NMOS branch of the gate can drawn as the following with the corresponding graph, while considering the longest path for sizing purposes:

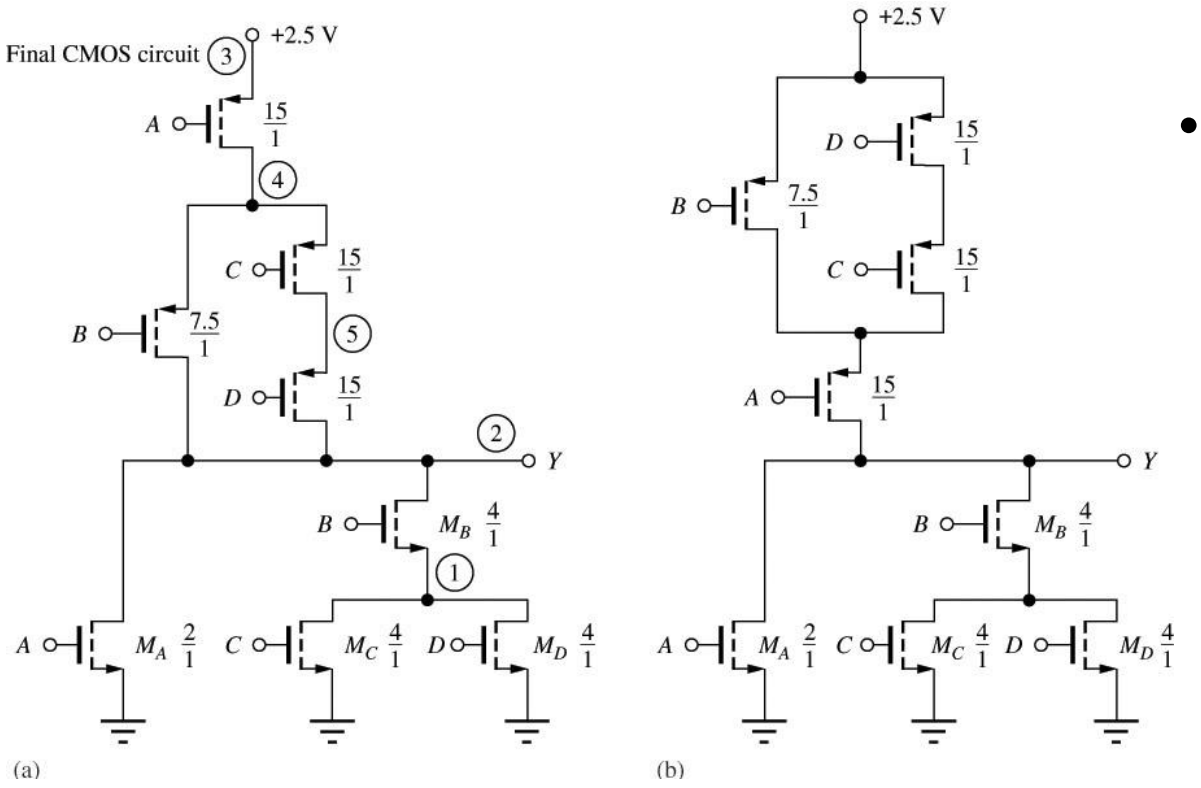


Complex CMOS Logic Gate Design Example

- By placing nodes in the interior of each arc, plus two more outside the graph for V_{DD} (3) and the complementary output (2'), the PMOS branch can be realized as shown on the left figure
- Connect all of the nodes in the manner shown in the right figure, and the NMOS arc's that the PMOS arc's intersect have the same inputs



Complex CMOS Logic Gate Design Example

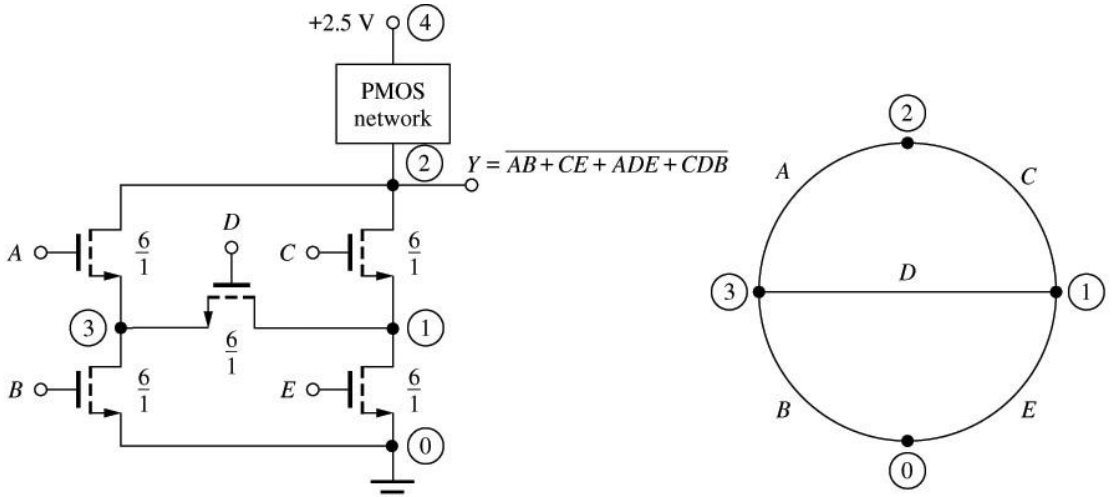


Two equivalent forms of the final circuit

- From the PMOS graph, the PMOS network can now be drawn for the final CMOS logic gate while once again considering the longest PMOS path for sizing

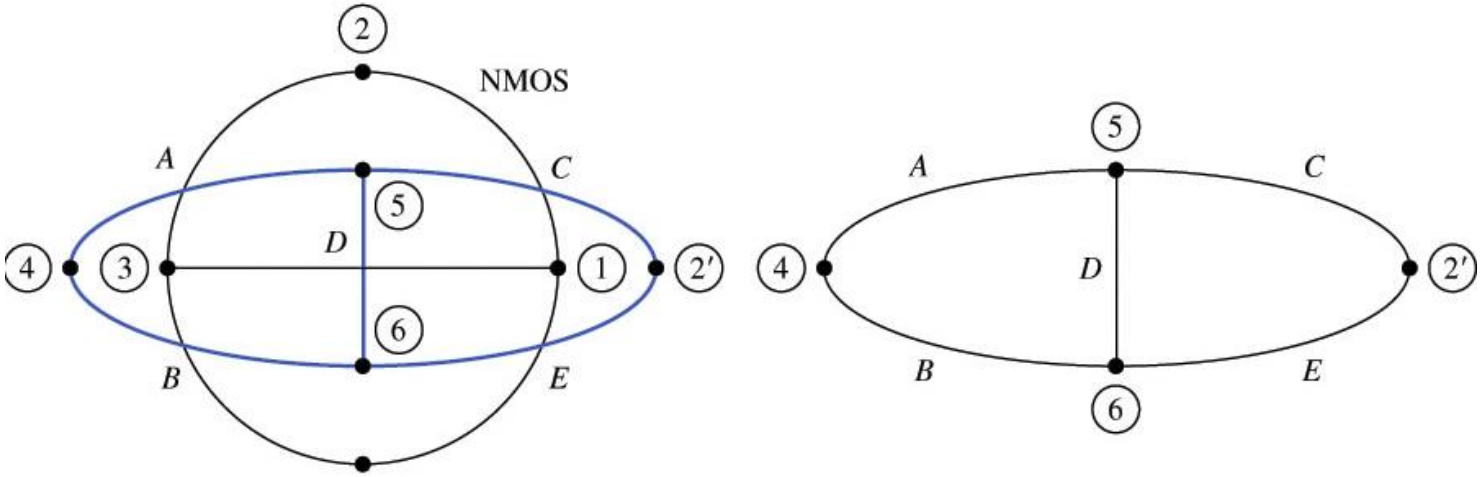
Complex CMOS Gate with a Bridging Transistor - Design Example

- Design a CMOS gate that implements the following logic function using the same reference inverter sizes as the previous example:
  $Y = \overline{AB + CE + ADE + CDB}$
- The NMOS branch can be realized in the following manner using bridging NMOS D to implement $\overline{Y}$. The corresponding NMOS graph is shown to the right.

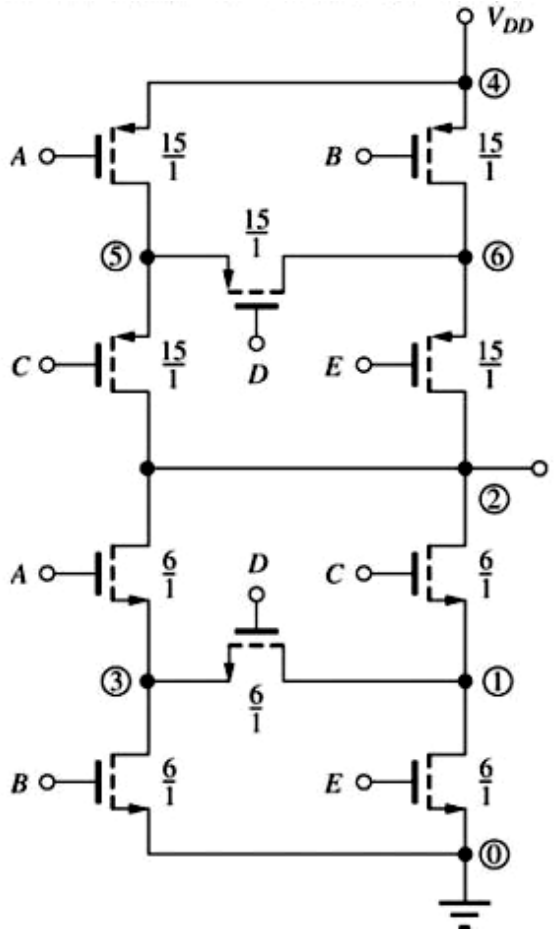


Complex CMOS Gate with a Bridging Transistor - Design Example

- By using the same technique as before, the PMOS graph can now be drawn



Complex CMOS Gate with a Bridging Transistor - Design Example



- By using the PMOS graph, the PMOS network can now be realized as shown (considering the longest path for sizing)

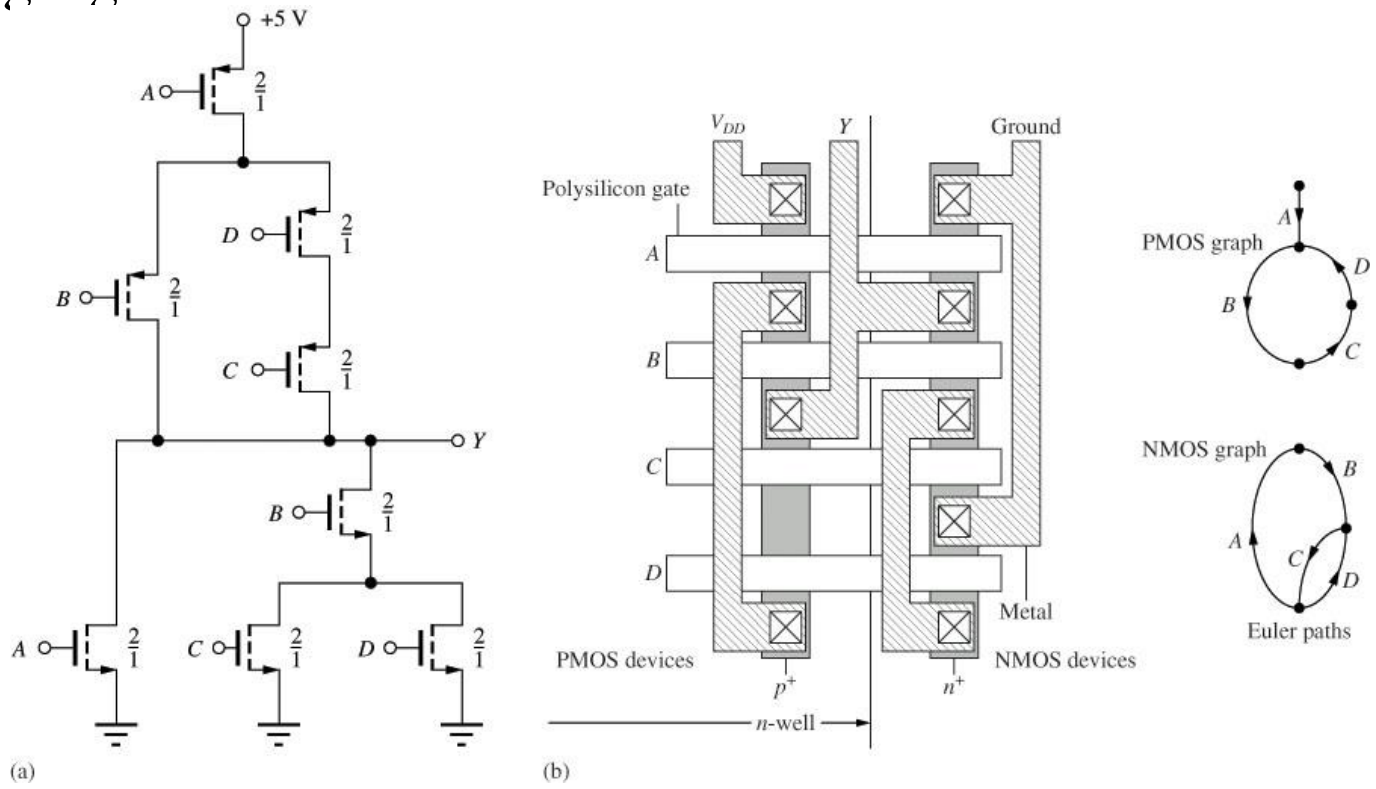
Minimum Size Gate Design and Performance

- With CMOS technology, there is an area/delay tradeoff that needs to be considered

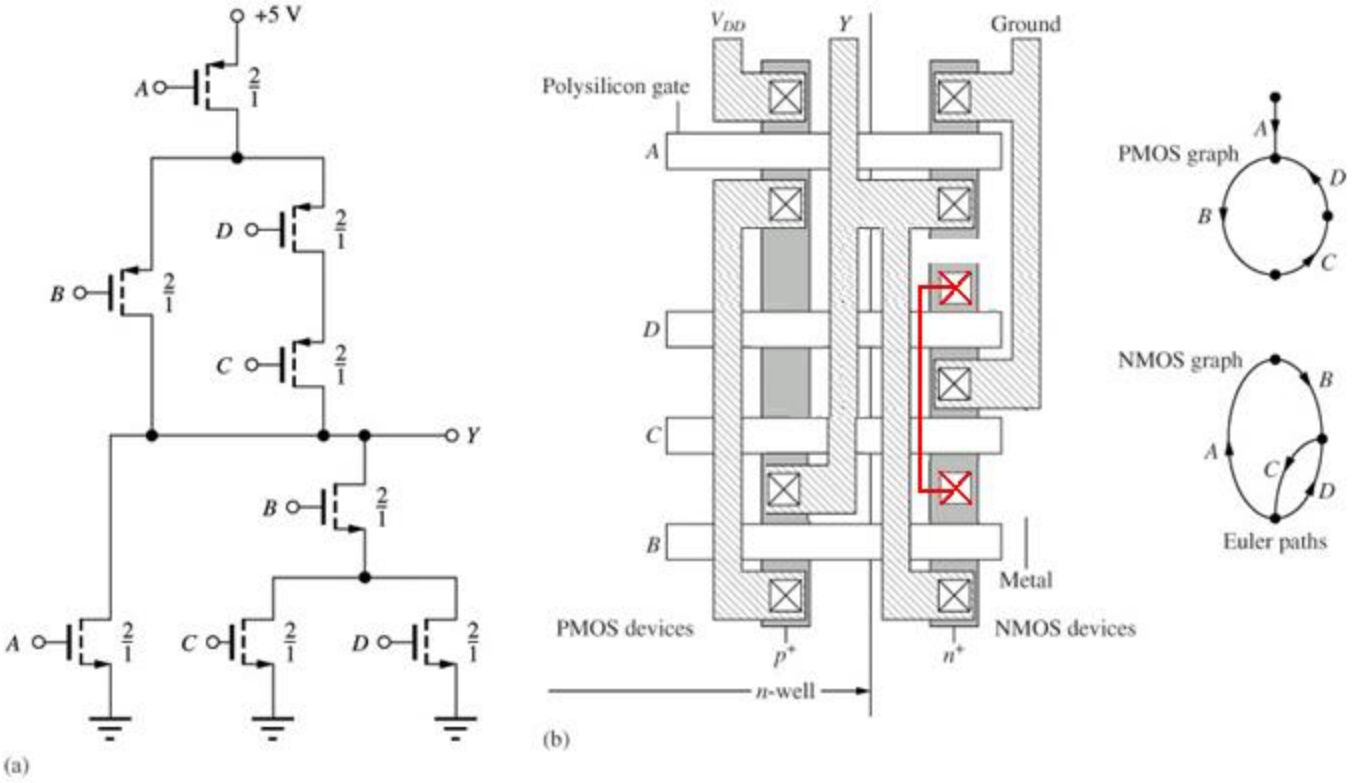
- If minimum feature sized are used for both devices, then the τ_{PLH} will be increased compared to the symmetrical reference inverter

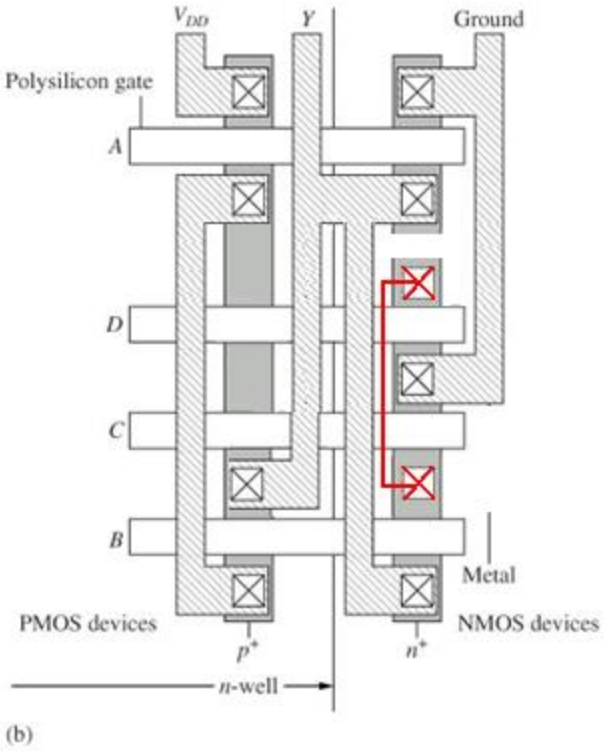
Minimum Size Complex Gate and Layout

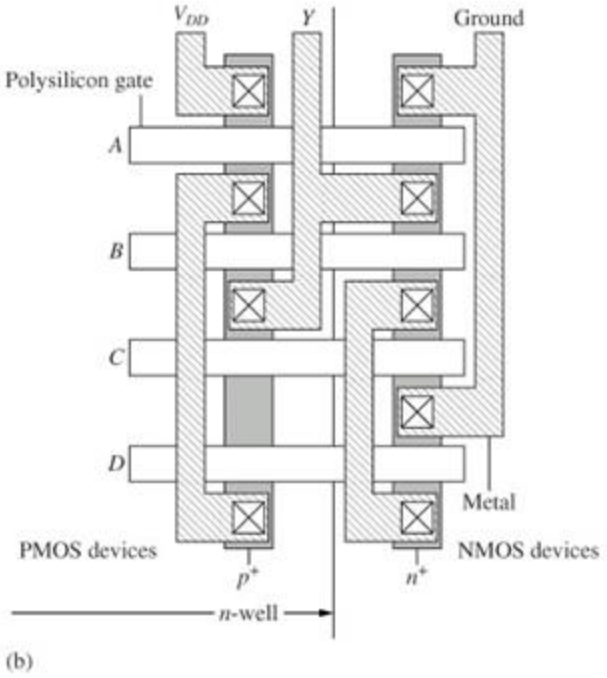
- The following shows the layout of a complex minimum size logic gate



Minimum Size Complex Gate and Layout




V_{DD}
Y
Ground
Polysilicon gate
A
D
C
B
Metal
PMOS devices
NMOS devices
p^+
n^+
n-well
(b)


V_{DD}
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