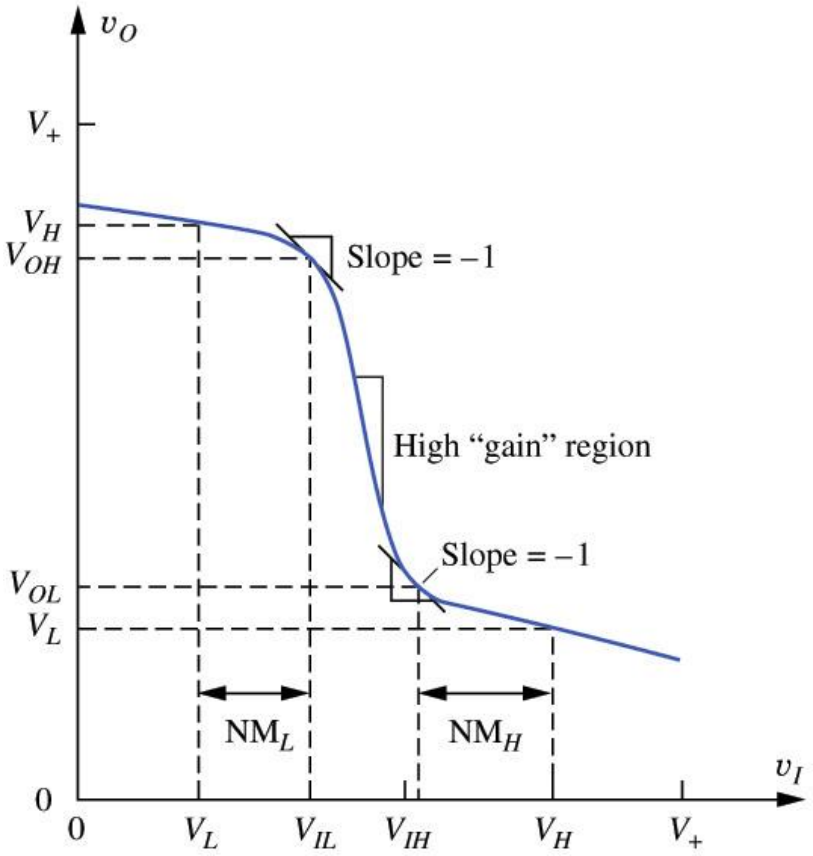
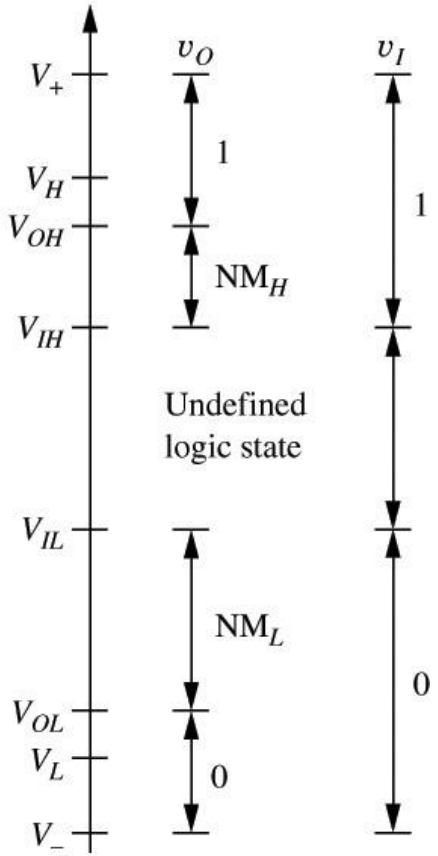
Logic Voltage Level Definitions

- V_L – The nominal voltage corresponding to a low-logic state at the output of a logic gate for $v_i = V_H$
- V_H – The nominal voltage corresponding to a high-logic state at the output of a logic gate for $v_i = V_L$
- V_{IL} – The maximum input voltage that will be recognized as a low input logic level
- V_{IH} – The minimum input voltage that will be recognized as a high input logic level
- V_{OH} – The output voltage corresponding to an input voltage of V_{IL}
- V_{OL} – The output voltage corresponding to an input voltage of V_{IH}

Logic Voltage Level Definitions (cont.)





Note that for the voltage transfer characteristic (VTC) of the nonideal inverter, there is now an undefined logic state.

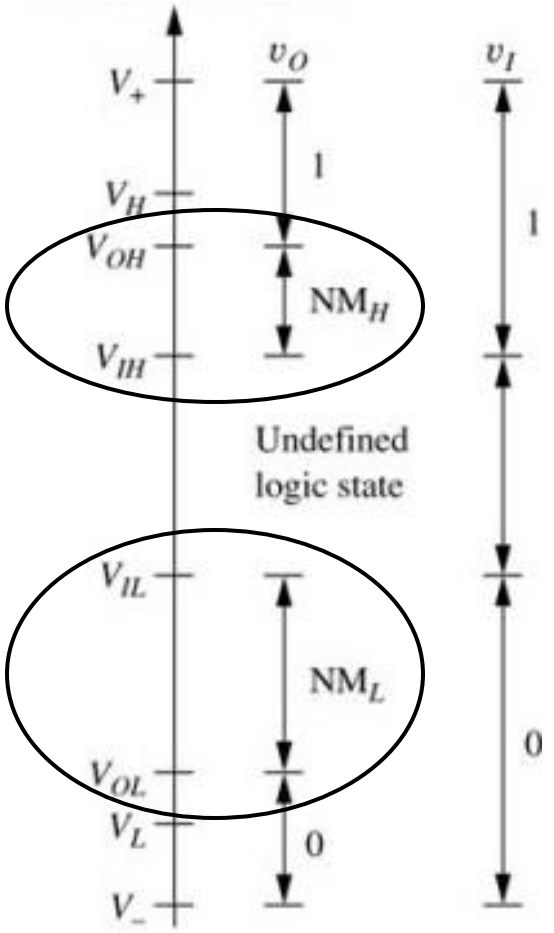
Noise Margins

- Noise margins represent "safety margins" that prevent the circuit from producing erroneous outputs in the presence of noisy inputs
- Noise margins are defined for low and high input levels using the following equations: one's output is the input of next stage

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

Noise Margins (cont.)



- Graphical representation of where noise margins are defined

Logic Gate Design Goals

- An ideal logic gate is highly nonlinear and attempts to quantize the input signal to two discrete states. In an actual gate, the designer should attempt to minimize the undefined input region while maximizing noise margins
- The input should produce a well-defined output, and changes at the output should have no effect on the input
- Voltage levels at the output of one gate should be compatible with the input levels of a following gate
- The gate should have sufficient fan-out and fan-in capabilities
- The gate should consume minimal power (and area for ICs) and still operate under the design specifications

Dynamic Response of Logic Gates

- An important figure of merit to describe logic gates is the response in the time domain
- The rise and fall times, t_f and t_r, are measured at the 10% and 90% points on the transitions between the two states as shown by the following expressions:

$$V_{10\%} = V_L + 0.1\Delta V$$

$$V_{90\%} = V_L + 0.9\Delta V = V_H - 0.1\Delta V$$

where ΔV is the logic swing given by $\Delta V = V_H - V_L$

Propagation Delay

- Propagation delay describes the amount of time between a the input reaching the 50% point and the output reaching the 50% point. The 50% point is described by the following:

$$V_{50\%} = \frac{V_H + V_L}{2}$$

- The high-to-low propagation delay, τ_{PHL}, and the low-to-high propagation delay, τ_{PLH}, are usually not equal, but can be combined as an average value:

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

Υπολογισμός delay αλλαγής στάθμης

- Ποιά είναι η αλλαγή του φορτίου πυκνωτή C οταν αλλάζει η τάση κατα ΔV ?

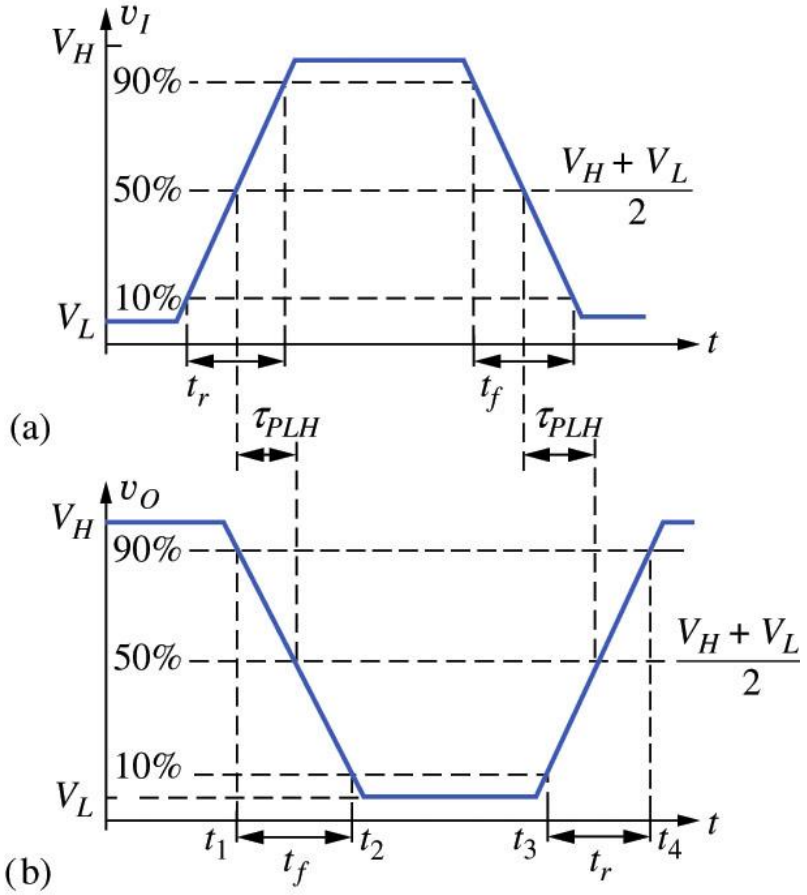
$$\Delta Q = C*(\Delta V)$$

Επειδή $dQ(t)/dt = I(t)$

τότε ο χρόνος Δt που απαιτείται για την αλλαγή του φορτίου είναι κατα προσέγγιση

$\Delta Q(t)/\Delta t$ = μέσο ρεύμα = I_m

Dynamic Response of Logic Gates



Power Delay Product

- The power-delay product (PDP) is used as a metric to describe the amount of energy (Joules) required to perform a basic logic operation and is given by the following equation where P is the average power dissipated by the logic gate:

$$PDP = P * \tau_{\mathrm{P}}$$

Review of Boolean Algebra (11/7)

A	Z
0	1
1	0

NOT
Truth Table

$Z = \overline{A}$

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

OR
Truth Table

$Z = A + B$

A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

AND
Truth Table

$Z = AB$

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

NOR
Truth Table

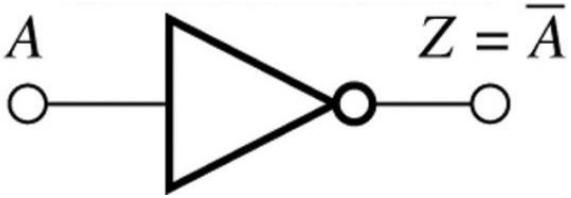
$Z = \overline{A + B}$

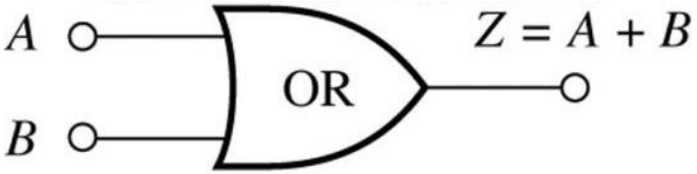
A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

NAND
Truth Table

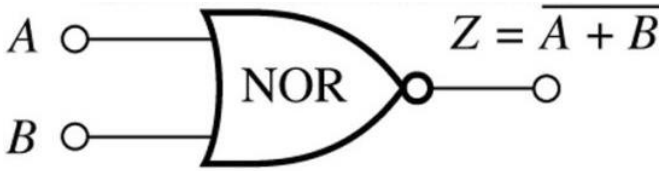
$Z = \overline{AB}$

Logic Gate Symbols and Boolean Expressions

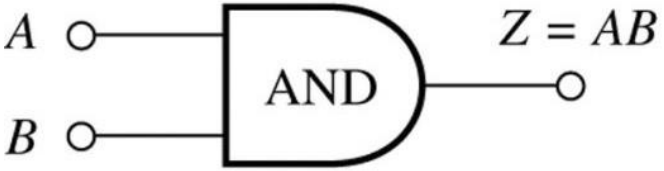




(a)



(a)

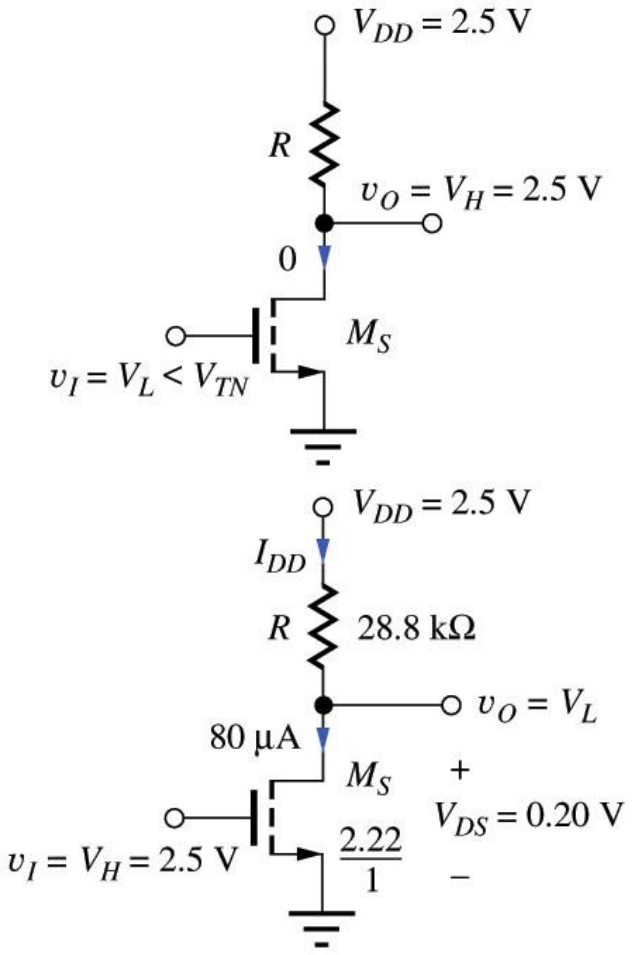


NMOS Logic Design

- MOS transistors (both PMOS and NMOS) can be combined with resistive loads to create single channel logic gates

- The circuit designer is limited to altering circuit topology and the width-to-length (W/L) ratio since the other factors are dependent upon processing parameters

NMOS Inverter with a Resistive Load



- The resistor R is used to "pull" the output high
- M_S is the switching transistor used to "pull" the output low
- The size of R and the W/L ratio of M_S are the design factors that need to be chosen

NMOS Model Summary

For all regions,

$$K_n = K_n' \frac{W}{L} \qquad K_n' = \mu_n C_{ox}'' \qquad i_G = 0 \qquad i_B = 0 \tag{4.24}$$

Cutoff region:

$$i_D = 0 \qquad \text{for } v_{GS} \leq V_{TN} \tag{4.25}$$

Triode region:

$$i_D = K_n \left(v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS} \qquad \text{for } v_{GS} - V_{TN} \geq v_{DS} \geq 0 \tag{4.26}$$

Saturation region:

$$i_D = \frac{K_n}{2} (v_{GS} - V_{TN})^2 (1 + \lambda v_{DS}) \qquad \text{for } v_{DS} \geq (v_{GS} - V_{TN}) \geq 0 \tag{4.27}$$

Threshold voltage:

$$V_{TN} = V_{TO} + \gamma \left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F} \right) \tag{4.28}$$

PMOS Model Summary

For all regions,

$$K_p = K'_p \frac{W}{L} \qquad K'_p = \mu_p C''_{\text{ox}} \qquad i_G = 0 \qquad i_B = 0 \tag{4.29}$$

Cutoff region:

$$i_D = 0 \qquad \text{for } V_{GS} \geq V_{TP} \tag{4.30}$$

Triode region:

$$i_D = K_p \left(v_{GS} - V_{TP} - \frac{v_{DS}}{2} \right) v_{DS} \qquad \text{for } 0 \leq |v_{DS}| \leq |v_{GS} - V_{TP}| \tag{4.31}$$

Saturation region:

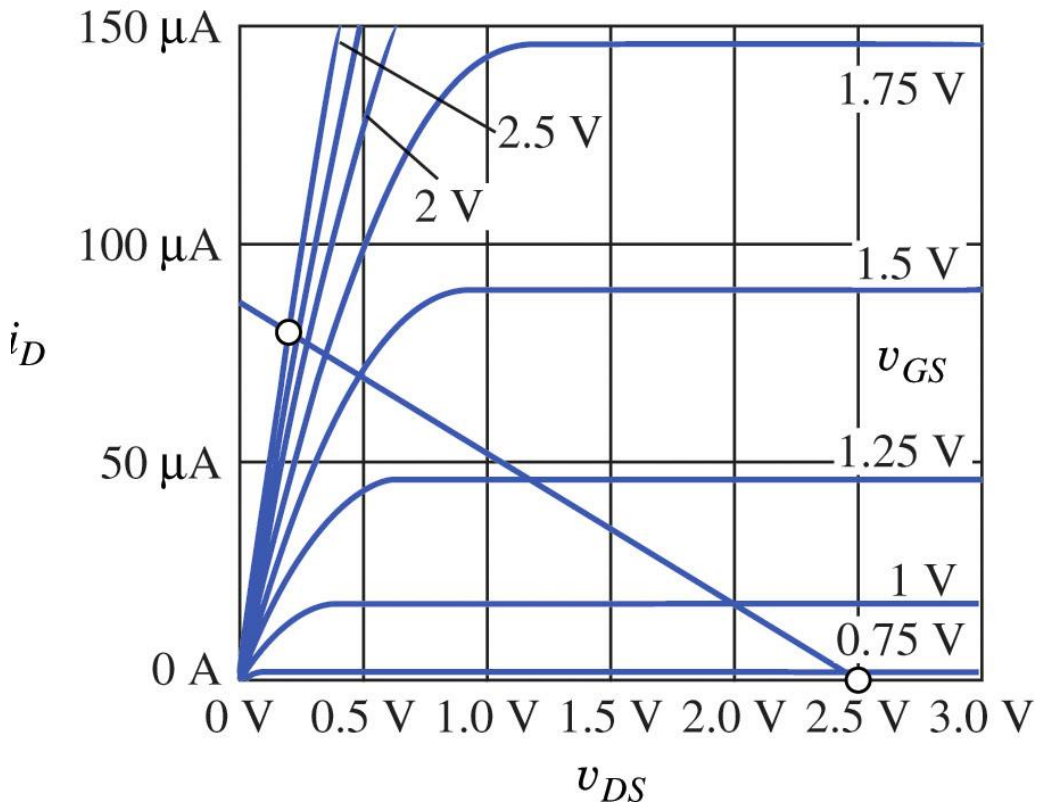
$$i_D = \frac{K_p}{2} (v_{GS} - V_{TP})^2 (1 + \lambda |v_{DS}|) \qquad \text{for } |v_{DS}| \geq |v_{GS} - V_{TP}| \geq 0 \tag{4.32}$$

Threshold voltage:

$$V_{TP} = V_{TO} - \gamma \left(\sqrt{v_{BS} + 2\phi_F} - \sqrt{2\phi_F} \right) \tag{4.33}$$

For the enhancement-mode PMOS transistor, $V_{TP} < 0$. Depletion-mode PMOS devices can also be fabricated; $V_{TP} \geq 0$ for these devices.

Load Line Visualization



The operation of the NMOS output (i_D, v_{DS}) characteristics.

Load line equation:

$$v_{DS} = V_{DD} - i_D R$$

NMOS with Resistive Load Design Example

- Design a NMOS resistive load inverter for
  - $V_{DD} = 3.3$ V
  - P = 0.1 mW when $V_L = 0.2$ V
  - $K_n = 60\ \mu A/V^2$
  - $V_{TN} = 0.75$ V

- Find the value of the load resistor R and the W/L ratio of the switching transistor M_S

Example continued

- First the value of the current through the resistor (for $v_O = V_L$) must be determined by using the following:

$$I_{DD} = \frac{P}{V_{DD}} = \frac{0.1mW}{3.3V} = 30.3\mu A$$

- The value of the resistor can now be found by the following which assumes that the transistor is on and the output is low:

$$R = \frac{V_{DD} - V_L}{I_{DD}} = \frac{3.3V - 0.2V}{30.3\mu A} = 102k\Omega$$

Example Continued

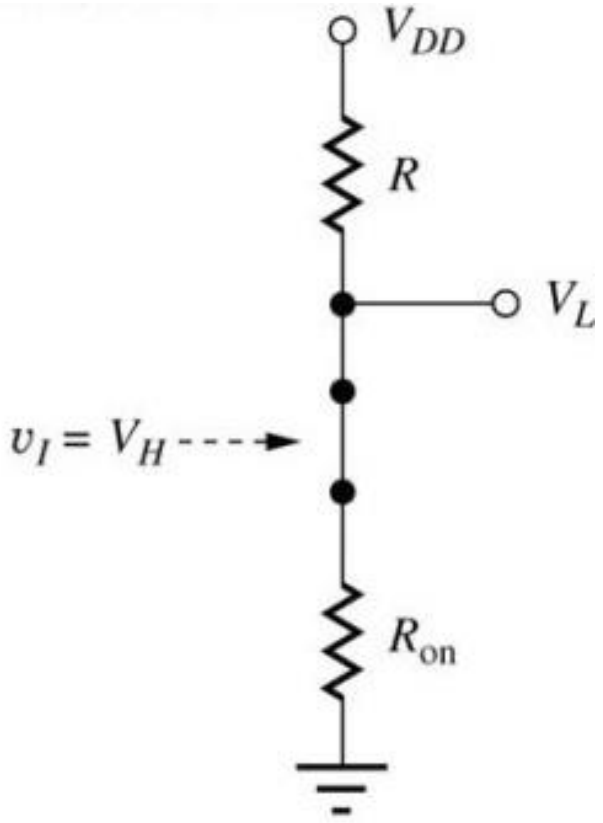
- For $v_I = V_H = 3.3$ V, and $v_O = V_L = 0.2$V, the transistor's drain-source voltage V_{DS} will be less than $V_{GS} - V_{TN}$. Therefore it will be operating in the triode region. Using the triode region equation for the MOSFET, the W/L ratio can be found:

$$I_D = K_n'\left(\frac{W}{L}\right)_S\left(V_H - V_{TN} - \frac{V_L}{2}\right)V_L$$

$$30.3\mu A = \left(60\times 10^{-6}\right)\left(\frac{W}{L}\right)_S\left(3.3 - 0.75 - \frac{0.2}{2}\right)0.2$$

$$\left(\frac{W}{L}\right)_S = \frac{1.03}{1} \cong \frac{1}{1}$$

On-Resistance of the Switching Device, M_S



- The NMOS resistive load inverter can be thought of as a resistive divider when the output is low, described by the following expression:

$$V_L = V_{DD}\frac{R_{on}}{R_{on}+R}$$

On-Resistance of M_S (cont.)

When the NMOS resistive load inverter's output is low, the On-Resistance R_{on} of the NMOS can be calculated with the following expression:

$$R_{on} = \frac{v_{DS}}{i_D} = \frac{1}{K_n'\left(\frac{W}{L}\right)\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)}$$

Note that R_{on} should be kept small compared to R to ensure that V_L remains low, and also that its value is nonlinear, since it has a dependence on v_{DS}

Calculation of V_{IL} and V_{OH}

Our analysis begins with the expression for the load line, repeated here from Eq. (6.8):

$$v_O = V_{DD} - i_D R \tag{6.14}$$

Referring to Fig. 6.15 with $v_I = V_{IL}$, v_{GS} is small and v_{DS} is large, so we expect the MOSFET to be operating in saturation, with drain current given by

$$i_D = (K_n/2)(v_{GS} - V_{TN})^2 \qquad \text{where } K_n = K_n'(W/L) \text{ and } v_{GS} = v_I$$

Substituting this expression for i_D in load-line Eq. (6.14),

$$v_O = V_{DD} - \frac{K_n}{2}(v_I - V_{TN})^2 R \tag{6.15}$$

and taking the derivative of v_O with respect to v_I results in

$$\frac{dv_O}{dv_I} = -K_n(v_I - V_{TN})R \tag{6.16}$$

Setting this derivative equal to -1 for $v_I = V_{IL}$ yields

$$V_{IL} = V_{TN} + \frac{1}{K_n R} \qquad \text{with} \qquad V_{OH} = V_{DD} - \frac{1}{2K_n R} \tag{6.17}$$

Calculation of V_{IH} and V_{OL}

For $v_I = V_{IH}$, v_{GS} is large and v_{DS} is small, so we now expect the MOSFET to be operating in the triode region with drain current given by $i_D = K_n[v_{GS} - V_{TN} - (v_{DS}/2)]v_{DS}$. Substituting this expression for i_D into Eq. (6.14) and realizing that $v_O = v_{DS}$ yields

$$v_O = V_{DD} - K_n R\left(v_I - V_{TN} - \frac{v_O}{2}\right)v_O \qquad \text{or} \qquad \frac{v_O^2}{2} - v_O\left[v_I - V_{TN} + \frac{1}{K_n R}\right] + \frac{V_{DD}}{K_n R} = 0 \tag{6.18}$$

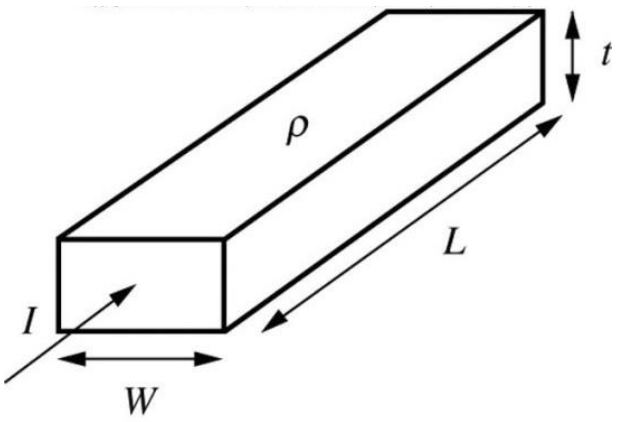
Solving for v_O and then setting $dv_O/dv_I = -1$ for $v_I = V_{IH}$ yields

$$V_{IH} = V_{TN} - \frac{1}{K_n R} + 1.63\sqrt{\frac{V_{DD}}{K_n R}} \qquad \text{with} \qquad V_{OL} = \sqrt{\frac{2V_{DD}}{3K_n R}} \tag{6.19}$$

Combining the results from Eqs. (6.17) and (6.19) yields expressions for the noise margins:

$$\text{NM}_H = V_{DD} - V_{TN} + \frac{1}{2K_n R} - 1.63\sqrt{\frac{V_{DD}}{K_n R}} \quad \text{and} \quad \text{NM}_L = V_{TN} + \frac{1}{K_n R} - \sqrt{\frac{2V_{DD}}{3K_n R}} \tag{6.20}$$

Load Resistor Problems

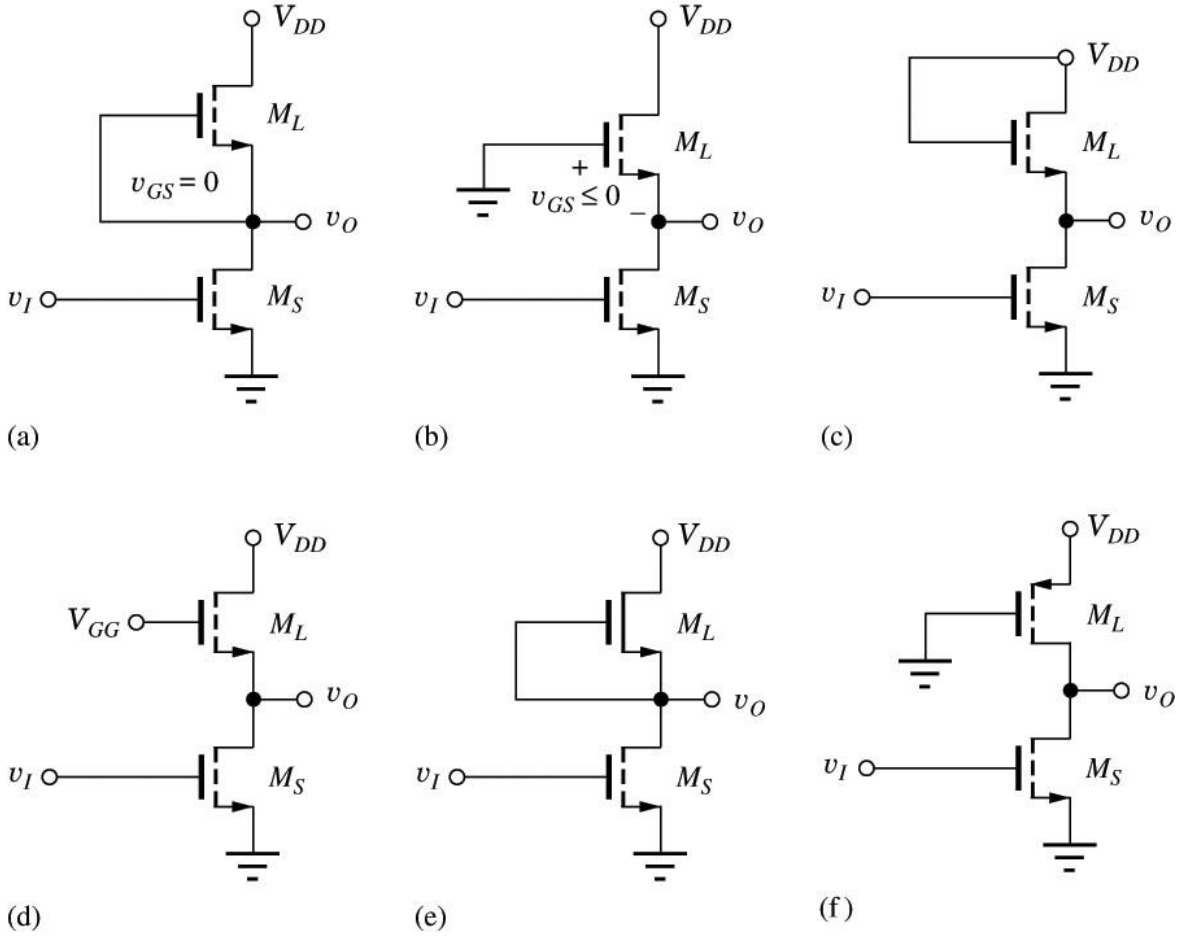


$$R = \frac{\rho L}{tW}$$

$$\frac{L}{W} = \frac{Rt}{\rho} = \frac{(95k\Omega)(1\times10^{-4}cm)}{0.001\Omega\cdot cm} = \frac{9500}{1}$$

- For completely integrated circuits, R must be implemented on chip using the shown structure
- Using the given equation, it can be seen that resistors take up a large area of silicon as in an example 95kΩ resistor

Using Transistors in Place of a Resistor



NMOS load with

a) gate connected to the source

b) gate connected to ground

c) gate connected to V_{DD}

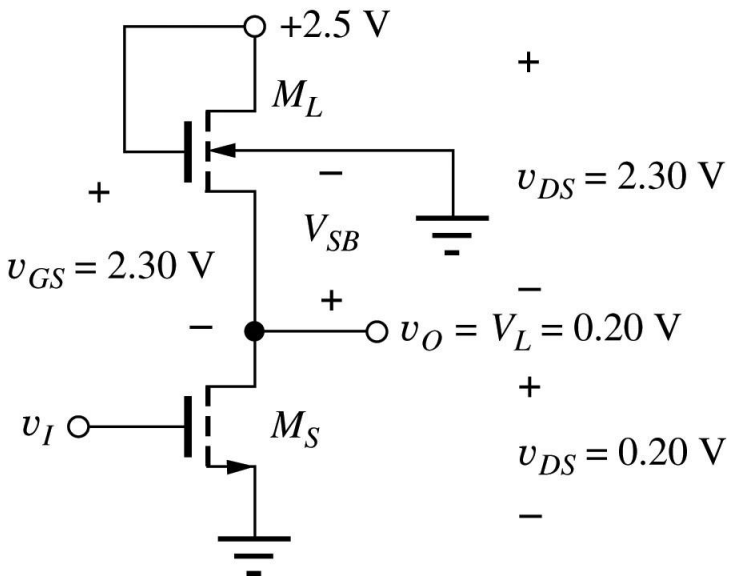
d) gate biased to linear region

e) a depletion-mode NMOSFET

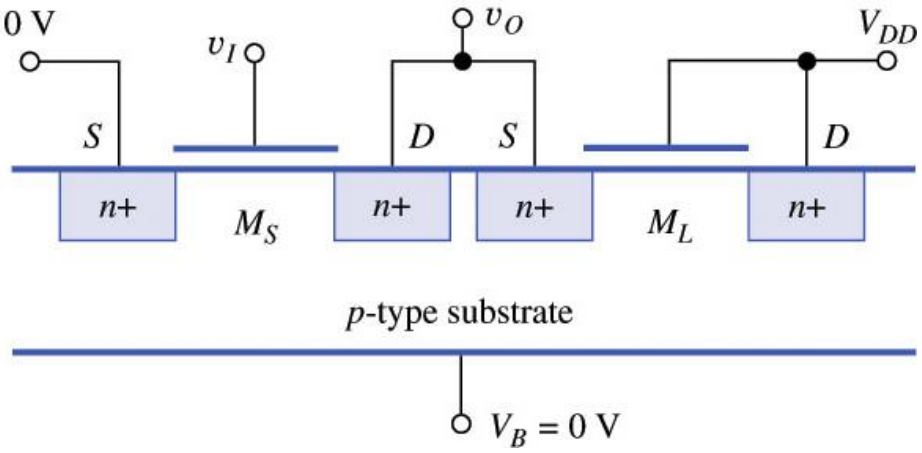
f) gate grounded PMOS load

Note that a) and b) are not useful. (M_L always off.)

Static Design of the NMOS Saturated Load Inverter



Schematic for a NMOS saturated load inverter



Cross-section for a NMOS saturated load inverter

Φαινόμενο σώματος

Το φαινόμενο σώματος (body effect) είναι η αιτία που αλλάζει την τάση κατωφλίου ενός MOSFET όταν η τάση V_{SB} γίνεται μεγαλύτερη από το μηδέν (0).

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$$

γ είναι η παράμετρος του φαινομένου σώματος (body effect parameter). Τυπική τιμή της παραμέτρου γ είναι 0.5 .
είναι το επιφανειακό δυναμικό (surface potential). Τυπική τιμή της παραμέτρου είναι $0.6V$.

NMOS Saturated Load Inverter Design Strategy

- Given V_{DD}, V_L, and the power level, find I_{DD} from V_{DD} and power
- Assume M_S off, and find high output voltage level V_H
- Use the value of V_H for the gate voltage of M_S and calculate $(W/L)_S$ of the switching transistor based on the design values of I_{DD} and V_L
- Find $(W/L)_L$ (load transistor) based on I_{DD} and V_L
- Check the operating region assumptions of M_S and M_L for $v_o = V_L$
- Verify design with a SPICE simulations

NMOS Saturated Load Inverter Design Example

- Design an saturated load inverter given the following specifications:

$$V_{DD} = 3.3V \qquad K_n^{'} = 50\mu A/V^2$$

$$V_L = 0.2V \qquad V_{TO} = 0.75V$$

$$I_{DD} = 60\mu A \qquad \gamma = 0.5\sqrt{V}$$

$$2\phi_F = 0.6V$$

NMOS Saturated Load Inverter Design Example

- First find V_H

$$V_H = V_{DD} - V_{TNL} = V_{DD} - \left[V_{TO} + \gamma\left(\sqrt{V_H + 2\phi_F} - \sqrt{2\phi_F}\right)\right]$$

$$V_H = 3.3 - \left[0.75 + 0.5\left(\sqrt{V_H + 0.6} - \sqrt{0.6}\right)\right]$$

$$V_H = 2.11V, \sout{4.01V}$$

(The output cannot exceed the positive power supply voltage.)

NMOS Saturated Load Inverter Design Example (11/14)

$$I_{DS} = K_n\left(\frac{W}{L}\right)_S\left(V_H - V_{TN} - \frac{V_L}{2}\right)V_L$$

$$60\mu A = \left(50\times10^{-6}\right)\left(\frac{W}{L}\right)_S\left(2.11 - 0.75 - \frac{0.2}{2}\right)0.2$$

$$\left(\frac{W}{L}\right)_S = \frac{4.76}{1}$$

$$I_{DL} = K_n\left(\frac{W}{L}\right)_L\left(V_{GSL} - V_{TNL}\right)^2$$

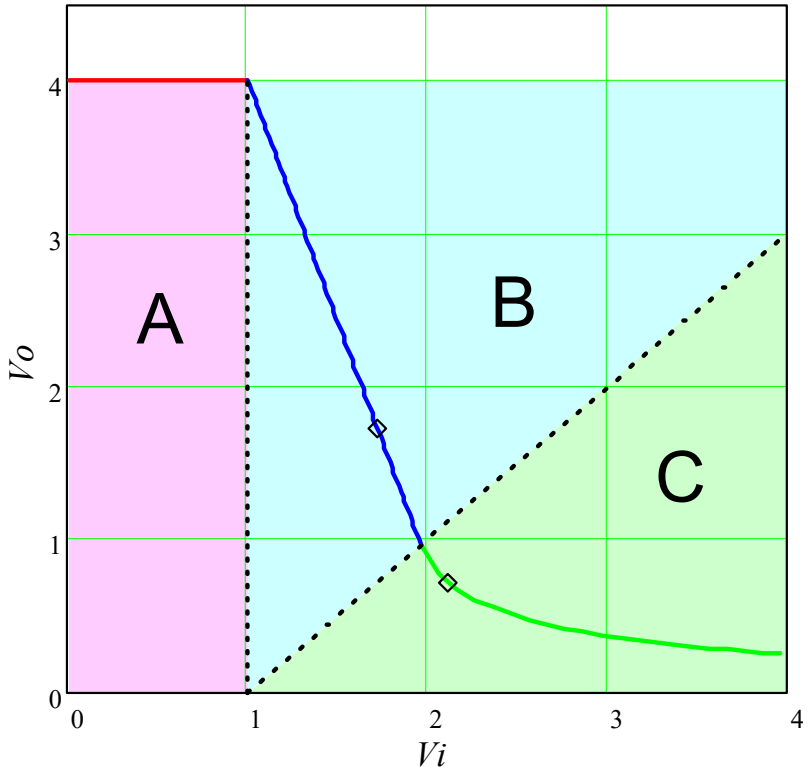
$$V_{TNL} = 0.75 + 0.5\left(\sqrt{0.2+0.6} - \sqrt{0.6}\right) = 0.81V$$

$$60\mu A = \left(50\times10^{-6}\right)\left(\frac{W}{L}\right)_L\left(3.3 - 0.2 - 0.81\right)^2$$

$$\left(\frac{W}{L}\right)_L = \frac{1}{2.19}$$

- For $v_o = V_L$, M_S is on (in the triode region), and M_L is in saturation.
- Find the W/L ratios of the two transistors

Περιοχές λειτουργίας αναστροφέα με saturated load



$V_{DD} = 5V$
$V_T = 1V$
$K_n' = \mu_n C_{OX} = 25\mu A/V^2$

Περιοχή	M_S	M_L	Συνθήκη
A	OFF	SAT	$Vi < V_T = 1V$
B	SAT	SAT	$Vi > V_T = 1V$ & $Vo > Vi - V_T$
C	LIN	SAT	$Vo < Vi - V_T$

Saturated load Inverter- περιοχή Β

Στη περιοχή αυτή έχουμε και τα δύο MOSFETS σε κατάσταση SAT Το ρεύμα που ρέει από το τροφοδοτικό να περνά σε σειρά και από τα δύο MOSFETS, συνεπώς

$$I_D = I_{DL} = I_{DS} \rightarrow$$
$$K_L \left(V_{GS} - V_T\right)_L^2 = K_S \left(V_{GS} - V_T\right)_S^2 \rightarrow$$
$$\left(V_{DD} - Vo - V_T\right)^2 = K_R \left(Vi - V_T\right)^2 \rightarrow$$
$$Vo = V_{DD} - Vi \cdot \sqrt{K_R} + V_T \cdot \left(\sqrt{K_R} - 1\right)$$

Διαπιστώνουμε μία πρωτοβάθμια σχέση μεταξύ *Vi* και *Vo*. Η γραμμή της συνάρτησης αυτής κινείται στην περιοχή Β, είναι ευθεία (μπλε χρώμα) με κλίση που ισούται κατ' απόλυτη τιμή με την **τετραγωνική ρίζα του K_R.**
Αρχή γραμμής περιοχής Β: *(Vi, Vo)=(1V, 4V)*
Τέλος γραμμής περιοχής Β *(Vo=Vi-V_T), K_R=10: (Vi, Vo)=(1.961V, 0.961V)*

Saturated load Inverter- περιοχή C

M_S =LIN, M_L=SAT

$$I_D = I_{DS} = I_{DL} \rightarrow$$

$$K_S\left(2(V_{GS}-V_T)V_{DS}-V_{DS}^2\right) = K_L\left(V_{GS}-V_T\right)^2 \rightarrow$$

$$K_R\left(2(Vi-V_T)Vo-Vo^2\right) = \left(V_{DD}-Vo-V_T\right)^2$$

$$\frac{\partial\left(K_R\left(2(Vi-V_T)Vo-Vo^2\right)\right)}{\partial Vi} = \frac{\partial\left(\left(V_{DD}-Vo-V_T\right)^2\right)}{\partial Vi} \rightarrow$$

$$2K_R\left(Vo+(Vi-V_T)\frac{\partial Vo}{\partial Vi}-Vo\frac{\partial Vo}{\partial Vi}\right) = -2\left(V_{DD}-Vo-V_T\right)\frac{\partial Vo}{\partial Vi}$$

$$\boxed{\frac{\partial Vo}{\partial Vi} = \frac{-K_R Vo}{K_R\left(Vi-V_T\right)+\left(V_{DD}-V_T\right)-Vo\left(K_R+1\right)}}$$

Κέρδος τάσης αναστροφέα

Saturated load Inverter- περιοχή C

$$\frac{\partial Vo}{\partial Vi} = -1 = \frac{-K_R Vo}{K_R\left(Vi - V_T\right) + \left(V_{DD} - V_T\right) - Vo\left(K_R + 1\right)} \rightarrow$$

$$Vo = \frac{K_R\left(Vi - V_T\right) + \left(V_{DD} - V_T\right)}{2K_R + 1} = \frac{10 \cdot Vi - 6}{21}$$

Αντικαθιστούμε τη Vo στην εξίσωση ρευμάτων και λύνουμε ως προς Vi : $Vi = V_{IH} = 2.109V$

$$NM_L = V_{IL} - V_{OL} = 1V - 0.245V = 0.755V$$

$$NM_H = V_{OH} - V_{IH} = 4V - 2.109V = 1.891V$$

V_{OH}	4.000V
V_{IL}	1.000V
V_{IM}	1.721V
V_{IH}	2.109V
V_{OL}	0.245V
NM_L	0.755V
NM_H	1.891V

Ανάλυση Saturated load Inverter

Να ευρεθούν τα VH, VL για saturated load inverter

Δίνονται: $V_{DD} = 2.5V, (W/L)_S = 10/1, (W/L)_L = 2/1, Kn' = 100\ \mu A/V^2, V_{TO} = 0.60\ V, \gamma = 0.5\ \sqrt{V}, 2\varphi_F = 0.6V$

1. Εύρεση V_H

$$V_H = 2.5 - [0.60 + 0.5(\sqrt{V_H + 0.6} - \sqrt{0.6})] \qquad V_H^2 - 4.824V_H + 5.082 = 0 \quad \text{for which} \quad V_H = \cancel{3.27\ V}\ \text{or}\ 1.55\ \text{V}$$

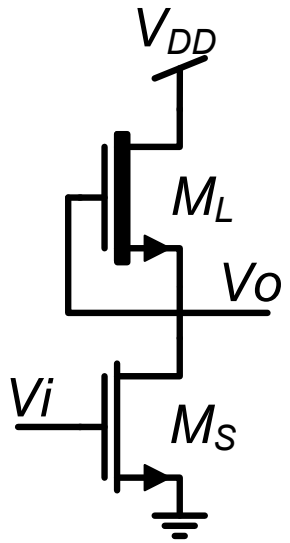
2. Εύρεση V_L

For $I_{DS} = I_{DL}$, we have $K_n' \left(\frac{10}{1}\right)\left(V_{GSS} - V_{TNS} - \frac{V_L}{2}\right)V_L = \frac{K_n'}{2}\left(\frac{2}{1}\right)(2.5 - V_L - V_{TNL})^2$ where

$$V_{TNL} = 0.60 + 0.5(\sqrt{V_L + 0.6} - \sqrt{0.6})$$

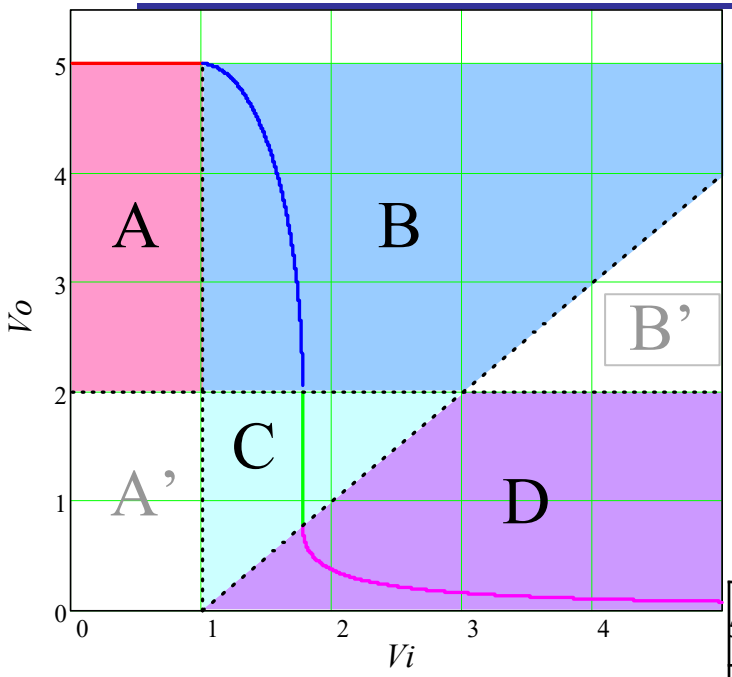
Προσέγγιση: Αγνοώ το body effect

Inverter με φορτίο Depletion MOSFET



Για το ***M***OSFET M_S που παίζει τον ρόλο του διακόπτη (***S****witch*) γνωρίζουμε ότι:
Όταν η *VGS*≤*VTE*, δηλαδή όταν *Vi*≤*VTE* τότε το *MS* είναι OFF.
Όταν η *VTE* ≤*VGS*≤*VDS*+*VTE*, δηλαδή όταν *VTE* ≤*Vi*≤*Vo*+*VTE* τότε το *MS* είναι SAT.
Όταν η *VTE* ≤*VGS*≥*VDS*+*VTE*, δηλαδή όταν *VTE* ≤*Vi*≥*Vo*+*VTE* τότε το *MS* είναι LIN.

Περιοχές λειτουργίας αναστροφέα με φορτίο Depletion MOSFET



$$V_{DD} = 5\text{V}$$
$$V_{TE} = 1\text{V}$$
$$V_{TD} = -3\text{V}$$
$$K_{n'} = \mu_n C_{OX} = 25\mu\text{A/V}^2$$

Περιοχή	M_S	M_L	Συνθήκη
A	OFF	LIN	$Vi<V_{TE}=1\text{V}$
B	SAT	LIN	$Vi> V_{TE}=1\text{V}$ και $Vo>V_{DD}+V_{TD}=2\text{V}$
C	SAT	SAT	$V_{DD}+V_{TD}=2\text{V}>Vo>Vi-V_{TE}$
D	LIN	SAT	$V_{DD}+V_{TD}=2\text{V}<Vo<Vi-V_{TE}$

Depletion load Inverter - περιοχή Β

- $V_{DD} = 5\text{V}$
- $V_{TE} = 1\text{V}$
- $V_{TD} = -3\text{V}$
- $K_n' = \mu_n C_{OX} = 25\mu\text{A/V}^2$

$$\frac{\partial Vo}{\partial Vi} = K_R \frac{(Vi - V_{TE})}{(V_{DD} - Vo + V_{TD})}$$

$$\frac{\partial Vo}{\partial Vi} = K_R \frac{(Vi - V_{TE})}{(V_{DD} - Vo + V_{TD})} = -1 \rightarrow$$

$$Vi = V_{TE} - \frac{V_{DD} - Vo + V_{TD}}{K_R}$$

$$Vi = V_{TE} - \frac{V_{TD}}{\sqrt{K_R(K_R + 1)}} = V_{IL} = 1.194V$$

Depletion load Inverter - περιοχή D

$$I_D = I_{DS} = I_{DL} \rightarrow$$

$$K_S\left(2\left(V_{GS} - V_{TD}\right)V_{DS} - V_{DS}^2\right) = K_L\left(V_{GS} - V_{TE}\right)^2 \rightarrow$$

$$K_R\left(2\left(Vi - V_{TE}\right)Vo - Vo^2\right) = \left(-V_{TD}\right)^2$$

$$\frac{\partial\left(K_R\left(2\left(Vi - V_{TE}\right)Vo - Vo^2\right)\right)}{\partial Vi} = \frac{\left(-V_{TD}\right)^2}{\partial Vi} \rightarrow$$

$$2K_R\left(Vo + \frac{\partial Vo}{\partial Vi}\left(Vi - V_{TE} - Vo\right)\right) = 0$$

$$\frac{\partial Vo}{\partial Vi} = \frac{-Vo}{\left(Vi - V_{TE}\right) - Vo}$$

$$Vi = V_{TE} - V_{TD}\sqrt{\frac{4}{3K_R}} = V_{IH} = 1.894V$$

Design of Depletion load Inverter

Known Information and Given Data: Circuit topology in Fig. 6.23; $V_{DD} = 3.3$ V, $P = 0.20$ mW, $V_L = 0.20$ V, $K_n' = 100\ \mu\text{A/V}^2$, $V_{TOS} = 0.60$ V, $V_{TOL} = -1$ V, $\gamma = 0.5\ \sqrt{\text{V}}$, and $2\phi_F = 0.6$ V for both transistor types

Unknowns: Power supply current I_{DD}, W/L ratios of the load and switching transistors M_S and M_L

Approach: Find V_H. Use V_H, I_{DD}, and the specified value of V_L to find $(W/L)_S$. Calculate V_{TNL}. Use I_{DD}, V_{TNL}, and the voltages in the circuit to find $(W/L)_L$.

$$V_{TNL} = -1 + 0.5(\sqrt{3.3 + 0.6} - \sqrt{0.6}) = -0.40\ \text{V} \quad \checkmark$$

Design of Depletion load Inverter

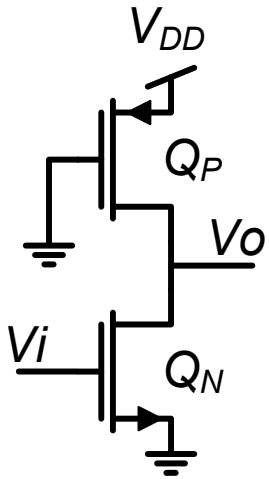
$$60.6\ \mu\text{A} = 100\ \mu\text{A}\left(\frac{W}{L}\right)_S\left(3.3 - 0.6 - \frac{0.20}{2}\right)0.20 \rightarrow \left(\frac{W}{L}\right)_S = \frac{1.17}{1}$$

In order to design the load transistor, we calculate its threshold voltage with $v_O = V_L = 0.20$ V, and then use V_{TNL} to find W/L (note that $V_{SB} = V_L = 0.20$ V):

$$V_{TNL} = -1 + 0.5\left(\sqrt{0.20 + 0.6} - \sqrt{0.6}\right) = -0.940\ \text{V}$$

$$60.6\ \mu\text{A} = \frac{100\ \mu\text{A}}{2}\left(\frac{W}{L}\right)_L(-0.94)^2 \rightarrow \left(\frac{W}{L}\right)_L = \frac{1.37}{1}$$

Pseudo NMOS Inverter (με φορτίο PMOS)



M_S (QN): off για $V_i < V_{TN}$, Sat για $V_o > V_i - V_{TN}$
ML (QP): Lin για $V_o > -V_{TP}$, Sat για $V_o < -V_{TP}$
(Sat για $|V_{DS}| > |V_{GS} - V_{TP}| \rightarrow |V_o - V_{DD}| > |-V_{DD} - V_{TP}|$)

Pseudo NMOS Inverter (με φορτίο PMOS)

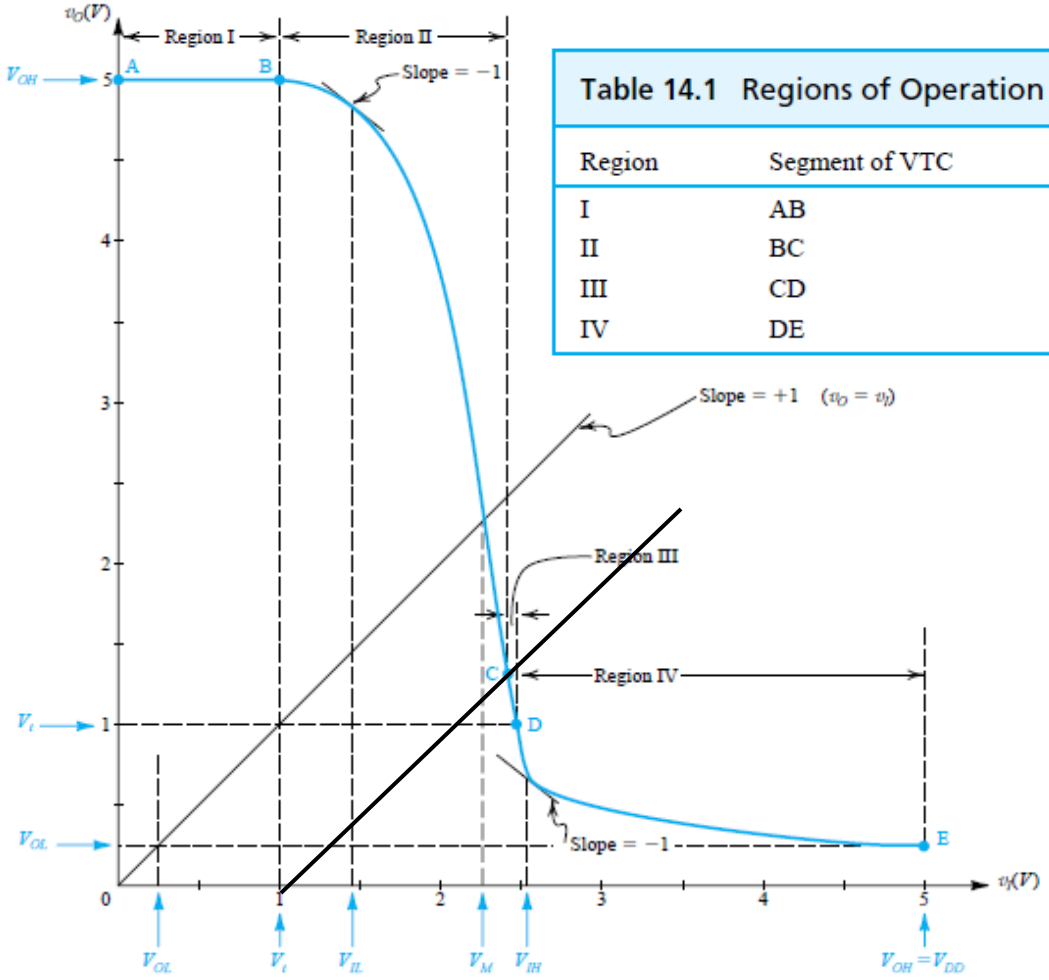


Table 14.1 Regions of Operation of the Pseudo-NMOS Inverter

Region	Segment of VTC	Q_N	Q_P	Condition
I	AB	Cutoff	Triode	$v_I < V_t$
II	BC	Saturation	Triode	$v_O \geq v_I - V_t$
III	CD	Triode	Triode	$V_t \leq v_O \leq v_I - V_t$
IV	DE	Triode	Saturation	$v_O \leq V_t$

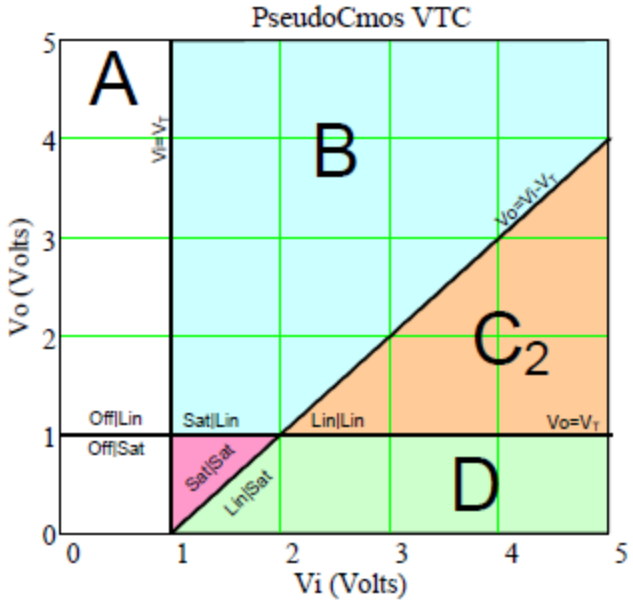


Figure 14.3 VTC for the pseudo-NMOS inverter. This curve is plotted for $V_{DD} = 5$ V, $V_{tn} = -V_{tp} = 1$ V, and $r = 9$.

Χαρακτηριστική Pseudo NMOS Inverter (I)

V_{DD}=5V, V_{TN}=-V_{TP}=1V, $\mu_n Cox$=50 μA/V^2, $\mu_p Cox$=30 μA/V^2

Περιοχή C

Όρια περιοχών C_1, C_2 = σημείο τομής δυο ευθειών

$$Vo = V_T \text{ και } Vo = Vi - V_T \rightarrow$$
$$Vi = 2V_T$$

$$I_{DP} = I_{DN} \rightarrow$$
$$(V_{DD} - V_T)^2 = K_R (Vi - V_T)^2 \rightarrow$$
$$K_R = \frac{(V_{DD} - V_T)^2}{(Vi - V_T)^2}$$

και σε συνδυασμό με την προηγούμενη περίπτωση

$$K_R = \left(\frac{V_{DD} - V_T}{V_T} \right)^2 = 16$$

Χαρακτηριστική Pseudo NMOS Inverter (II)

Περιοχή C_1

Όταν το K_R>16 τότε η χαρακτηριστική μεταφοράς περνά από την **περιοχή** C_1:

$$I_{DP} = I_{DN} \rightarrow$$

$$(V_{DD} - V_T)^2 = K_R (Vi - V_T)^2 \rightarrow$$

$$Vi = V_T + \frac{V_{DD} - V_T}{\sqrt{K_R}}$$

Περιοχή C_2

Όταν το K_R<16 τότε η χαρακτηριστική μεταφοράς περνά από την περιοχή C_2 όπου και τα δύο MOSFETs βρίσκονται στη γραμμική περιοχή λειτουργίας και συνεπώς:

$$I_{DP} = I_{DN} \rightarrow$$

$$2(V_{DD} - V_T)(V_{DD} - Vo) - (V_{DD} - Vo)^2 = K_R \left(2(Vi - V_T)Vo - Vo^2\right)$$

Pseudo NMOS Inverter (Design)

Υπολογισμός του $(W/L)_P$

For the PMOS device in Fig. 6.24, we see that $V_{GS} = -V_{DD}$, and the transistor will be in the conducting state. Since $V_{DS} = 0.2 - 2.5 = -2.3$ V and $V_{GS} - V_{TP} = -2.5 - (-0.6) = -1.9$ V, the transistor will be saturated ($|V_{DS}| > |V_{GS} - V_{TP}|$—see Section 4.2). We need to find the value of W/L that sets the PMOS drain current to 80 μA:

$$i_D = \frac{K_p'}{2}\left(\frac{W}{L}\right)_P (V_{GS} - V_{TP})^2 \qquad \text{or} \qquad 80\ \mu\text{A} = \frac{1}{2}\left(40\frac{\mu\text{A}}{V^2}\right)\left(\frac{W}{L}\right)_P [-2.5 - (-0.6)]^2 V^2$$

which gives $\left(\frac{W}{L}\right)_P = \frac{1.11}{1}$.

Υπολογισμός του $(W/L)_S$

drain current in the triode region of the device is used because $v_{GS} - V_{TN} = 2.5\text{ V} - 0.6\text{ V} = 1.9$ V, and $v_{DS} = V_L = 0.20$ V, yielding $v_{DS} < v_{GS} - V_{TN}$.

$$i_D = K_n'\left(\frac{W}{L}\right)_S (v_{GS} - V_{TN} - 0.5v_{DS})\, v_{DS} \qquad (6.10)$$

or

$$8 \times 10^{-5}\text{ A} = \left(100 \times 10^{-6}\frac{\text{A}}{\text{V}^2}\right)\left(\frac{W}{L}\right)_S (2.5\text{ V} - 0.6\text{ V} - 0.10\text{ V})(0.20\text{ V})$$

Solving Eq. (6.10) for $(W/L)_S$ gives $(W/L)_S = 2.22/1$.

Pseudo NMOS Inverter (Analysis)

Known Information and Given Data: Circuit topology in Fig. 6.26; $V_{DD} = 2.5$ V, $(W/L)_N = 10/1$, $(W/L)_P = 2/1$, $K_n' = 100\ \mu A/V^2$, $V_{TN} = 0.60$ V, $K_p' = 40\ \mu A/V^2$, and $V_{TP} = -0.60$ V.

$$K_n'\left(\frac{10}{1}\right)\left(V_{GSN} - V_{TN} - \frac{V_L}{2}\right)V_L = \frac{K_p'}{2}\left(\frac{2}{1}\right)(V_{GSP} - V_{TP})^2$$

$$100\frac{\mu A}{V^2}\left(\frac{10}{1}\right)\left(2.5 - 0.6 - \frac{V_L}{2}\right)V_L = \frac{40}{2}\frac{\mu A}{V^2}\left(\frac{2}{1}\right)(-2.5 - (-0.6))^2$$

$$12.5V_L^2 - 47.5V_L + 3.61 = 0 \qquad \text{for which} \qquad V_L = 0.0776\ \text{V}, \ \sout{3.72\ \text{V}}.$$

Έλεγχος λειτουργίας transistor (Q_N Lin, Q_P Sat ?)

Noise Margin για Pseudo NMOS (I)

Για V_{IL} : M_S=*Sat*, M_L= *Lin*

$$\frac{K_S}{2}(v_I - V_{TN})^2 = K_L\left(-V_{DD} - V_{TP} - \frac{v_O - V_{DD}}{2}\right)(v_O - V_{DD})$$

with

$$K_S = K_n'\left(\frac{W}{L}\right)_S \quad \text{and} \quad K_L = K_p'\left(\frac{W}{L}\right)_L$$

$$v_I = V_{TN} + \frac{1}{\sqrt{K_R}}\sqrt{[2(V_{DD} + V_{TP}) - (V_{DD} - v_O)](V_{DD} - v_O)} \quad \text{where} \quad K_R = \frac{K_S}{K_L}$$

$$V_{IL} = V_{TN} + \frac{(V_{DD} + V_{TP})}{\sqrt{K_R^2 + K_R}} \quad \text{and} \quad V_{OH} = V_{DD} - (V_{DD} + V_{TP})\left(1 - \sqrt{\frac{K_R}{K_R + 1}}\right)$$

Noise Margin για Pseudo NMOS (II)

Για V_{IH} : M_S=Lin, M_L= Sat

$$K_S\left(v_I - V_{TN} - \frac{v_O}{2}\right)v_O = \frac{K_L}{2}(-V_{DD} - V_{TP})^2$$

$$v_I = V_{TN} + \frac{v_O}{2} + \frac{(V_{DD} + V_{TP})^2}{2K_R}\left(\frac{1}{v_O}\right) \quad \text{where} \quad K_R = \frac{K_S}{K_L}$$

$$\frac{\partial v_I}{\partial v_O} = \frac{1}{2} - \frac{1}{2K_R}\frac{(V_{DD} + V_{TP})^2}{v_O^2}$$

$$V_{OL} = \frac{V_{DD} + V_{TNP}}{\sqrt{3K_R}} \qquad V_{IH} = V_{TN} + \frac{2(V_{DD} + V_{TP})}{\sqrt{3K_R}} = V_{TN} + 2V_{OL}$$

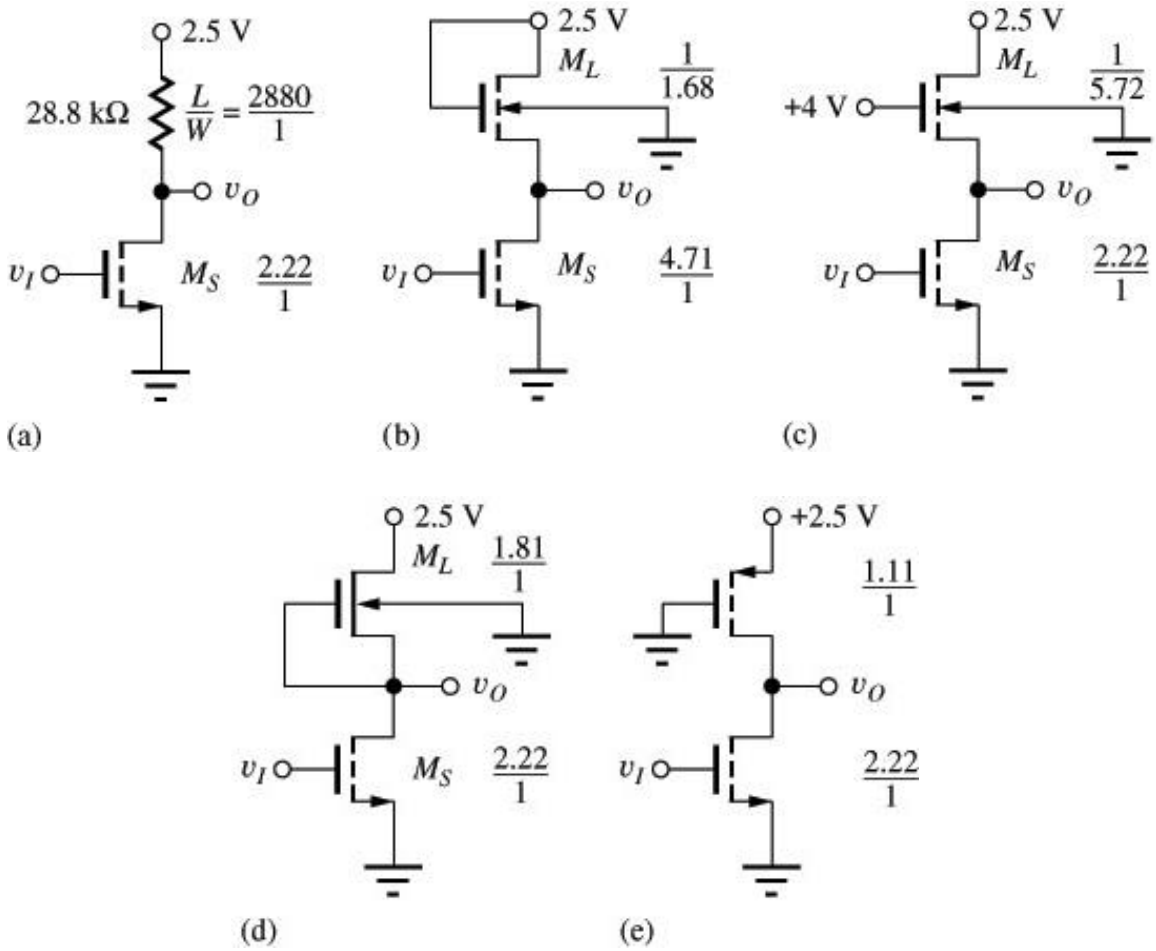
NMOS Inverter Summary

- Resistive load inverter takes up too much area for and IC design.
- The saturated load configuration is the simplest design, but V_H never reaches V_{DD}, and it has a slow switching speed.
- The linear load inverter fixes the speed and logic level issues, but it requires an additional power supply for the load gate.
- The depletion-mode NMOS load requires the most processing steps, but needs small area to achieve the high speed, $V_H = V_{DD}$, and best combination of noise margins.
- The Pseudo NMOS inverter offers the best speed with the lowest area.

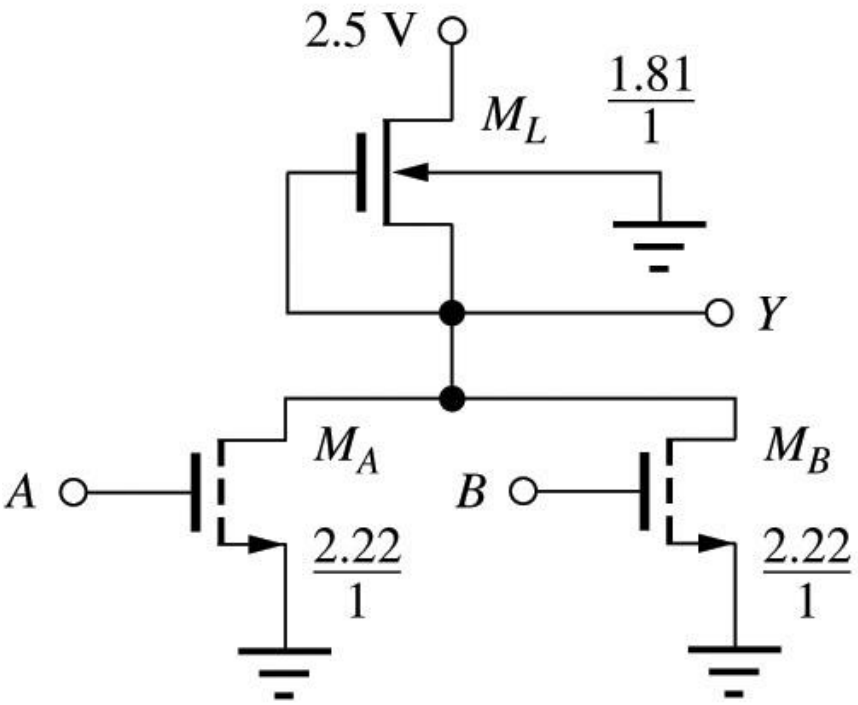
Typical Inverter Characteristics

	Inverter w/ Resistor Load	**Saturated Load Inverter**	**Linear Load Inverter**	**Inverter w/ Depletion-Mode Load**	**Pseudo-NMOS Inverter**
V_H (V)	2.50	1.55	2.50	2.50	2.50
V_L (V)	0.20	0.20	0.20	0.20	0.20
N_{ML} (V)	0.25	0.25	0.12	0.43	0.46
N_{MH} (V)	0.96	0.33	0.96	0.90	0.75
Relative Area	2880	6.39	7.94	4.03	3.33

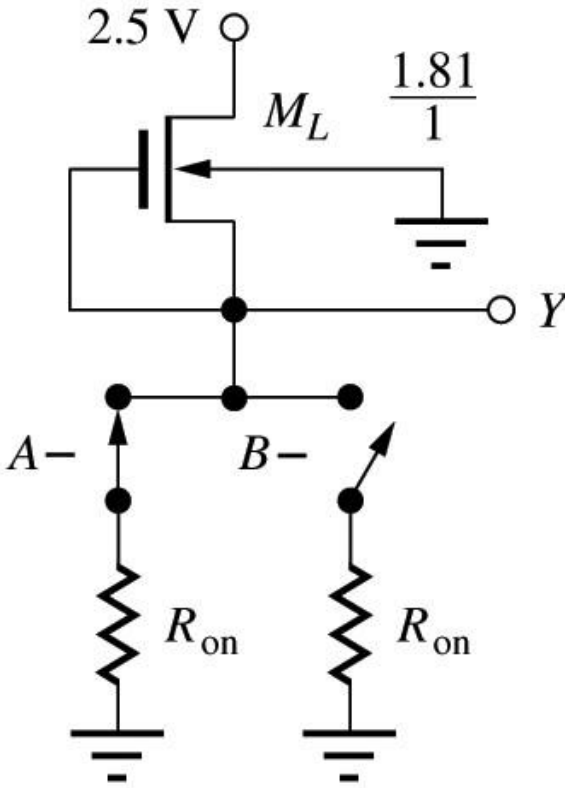
Reference Inverter Designs for Later Sections



NOR Gates

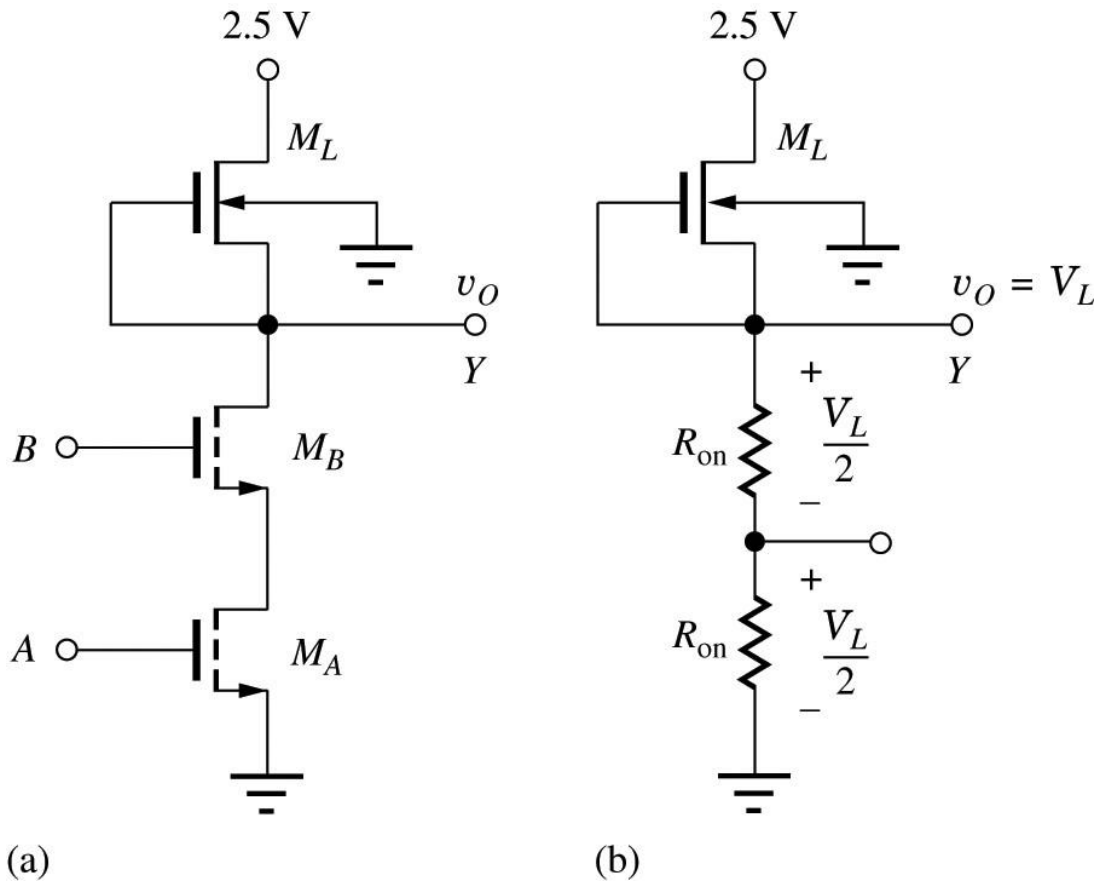


Two-input NOR gate



Simplified switch model for the NOR gate with M_A on

NAND Gates



Two-input NAND gate (left)

Simplified switch model for the NOR gate with A and B on (right)

NAND Gate Device Size Selection

- The NAND switching transistors can be sized based on the depletion-mode load inverter
- To keep the low voltage level comparable with the inverter, the desired R_{on} of M_A and M_B must be $0.5R_{on}$ of $M_{S,Inverter}$
- This can be accomplished by approximately doubling $(W/L)_A$ and $(W/L)_B$
- The sizes can also be chosen by using the design value of V_L and using the following equation:

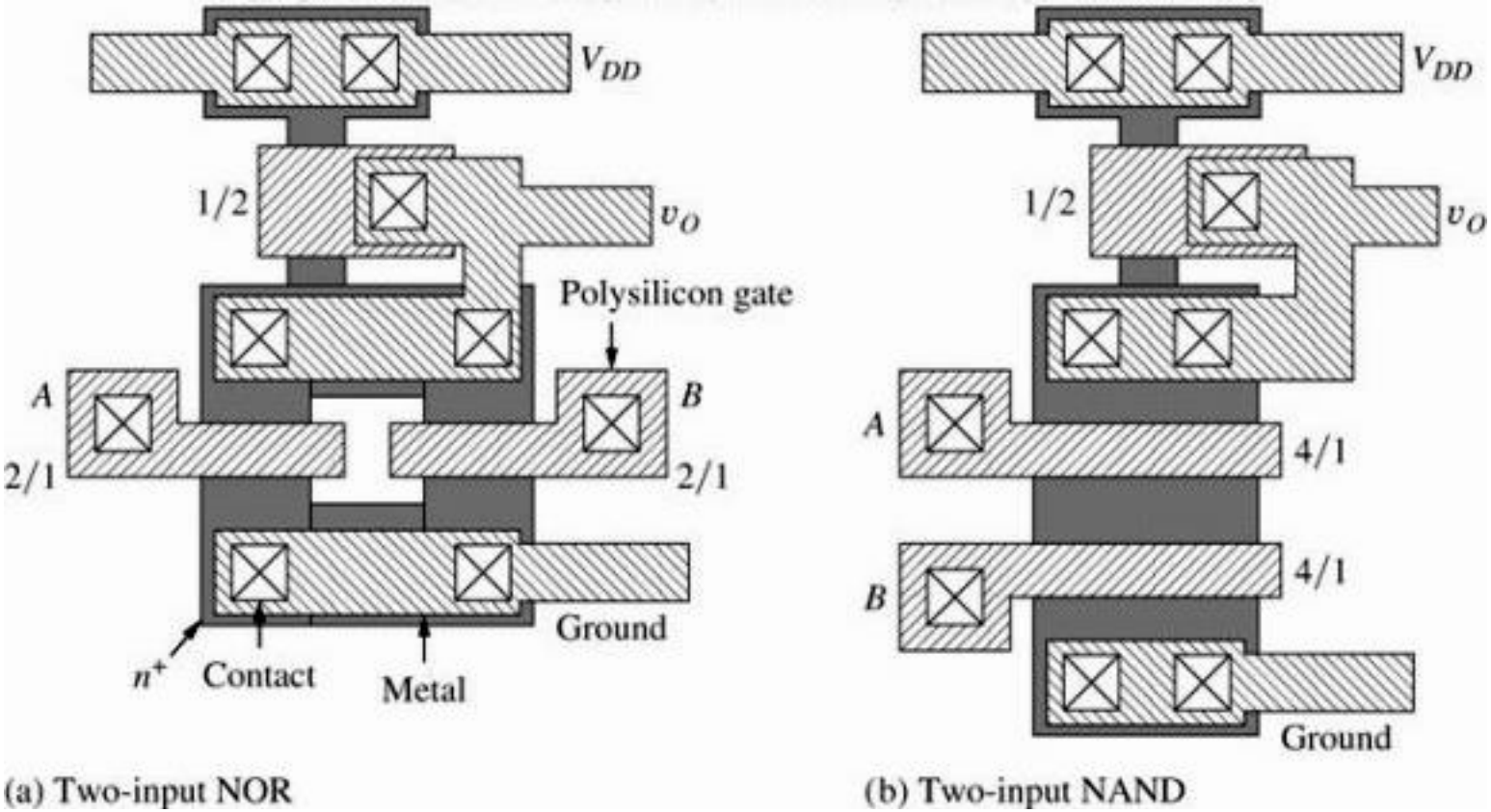
$$i_D = K_n'\left(\frac{W}{L}\right)_S\left(v_{GS} - V_{TN} - 0.5v_{DS}\right)v_{DS} \cong K_n'\left(\frac{W}{L}\right)_S\left(v_{GS} - V_{TN}\right)v_{DS}$$

NAND Gate Device Size Selection (cont.)

- Two sources of error that arise are the facts that the V_{SB}'s and V_{GS}'s of the two transistors are not equal. These factors should be considered for proper gate design

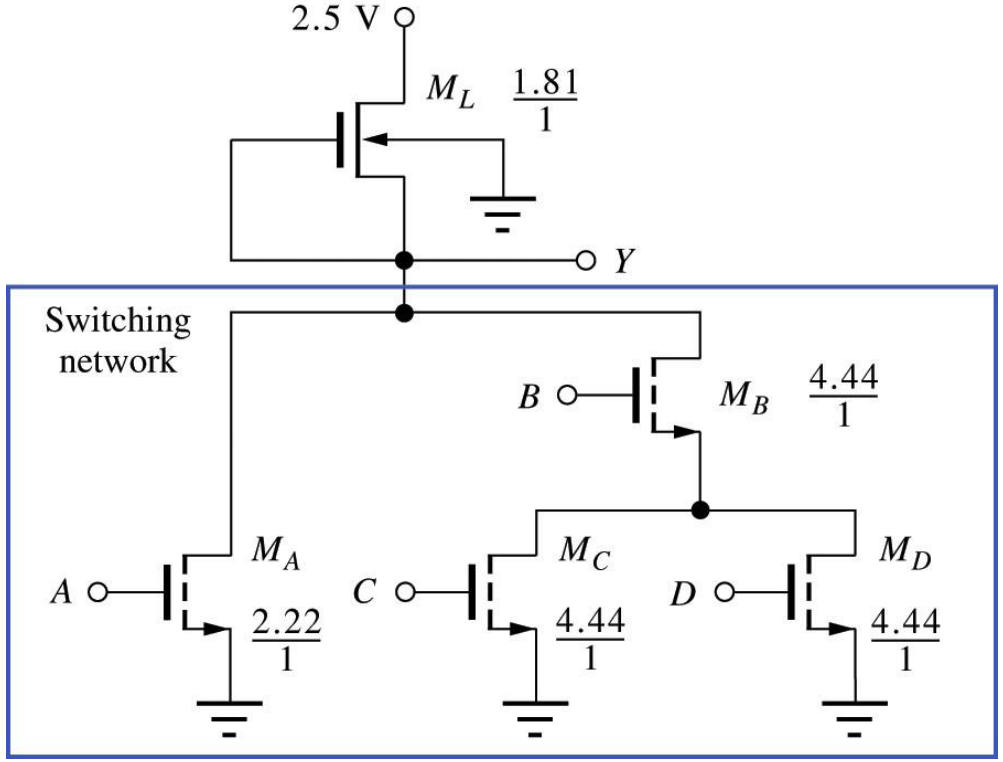
- The technique used to calculate the size of the load transistor for the NAND gate is exactly the same as for the depletion-load inverter

Layout of the NMOS Depletion-Mode NOR and NAND Gates



6.9 Complex NMOS Logic Design

An advantage of NMOS technology is that it is simple to design complex logic functions based on the NOR and NAND gates



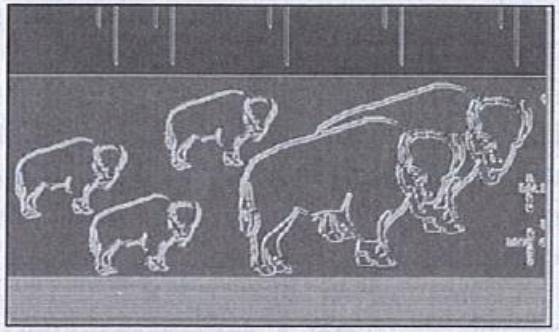
The circuit in the figure has the logic function:

$$Y = \overline{A + BC + BD}$$

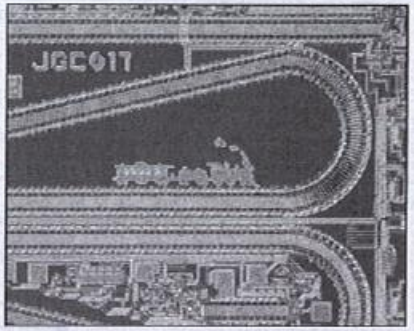
ELECTRONICS IN ACTION

Silicon Art

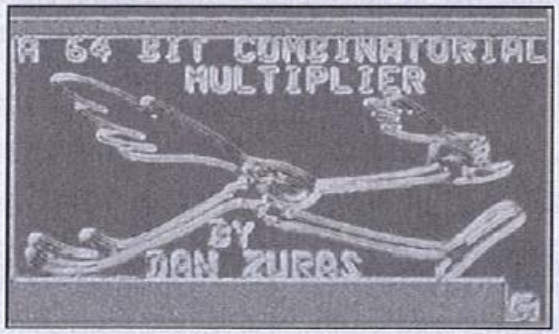
Successful integrated circuit designers are typically a very creative group of people. In the course of a large chip design project, engineers generate numerous innovations. The process involves many long hours leading up to the release of the chip layout data to manufacturing.



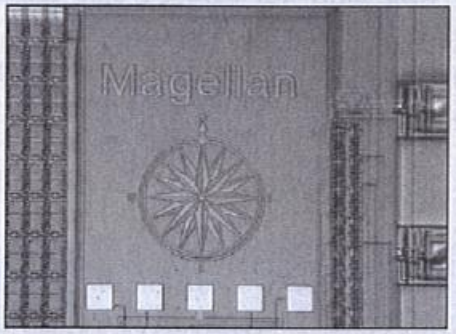
A small herd of buffalo added to a Hewlett-Packard 64-bit combinatorial divider created by HP engineer Dick Vlach.



A train found on an analog shift register from a LeCroy MVV200 integrated circuit.



A roadrunner drawn in aluminum on silicon by Dan Zuras of Hewlett-Packard.



A compass placed on a prototype optical navigation chip by Hewlett-Packard Labs designer Travis Blalock.

As the end of the design process nears, exhausted designers often want to add a more personal imprint on their work. Traditionally this has taken the form of using patterns in the metal layers of the chip layout to create graphical images relating to the chip's internal code name.

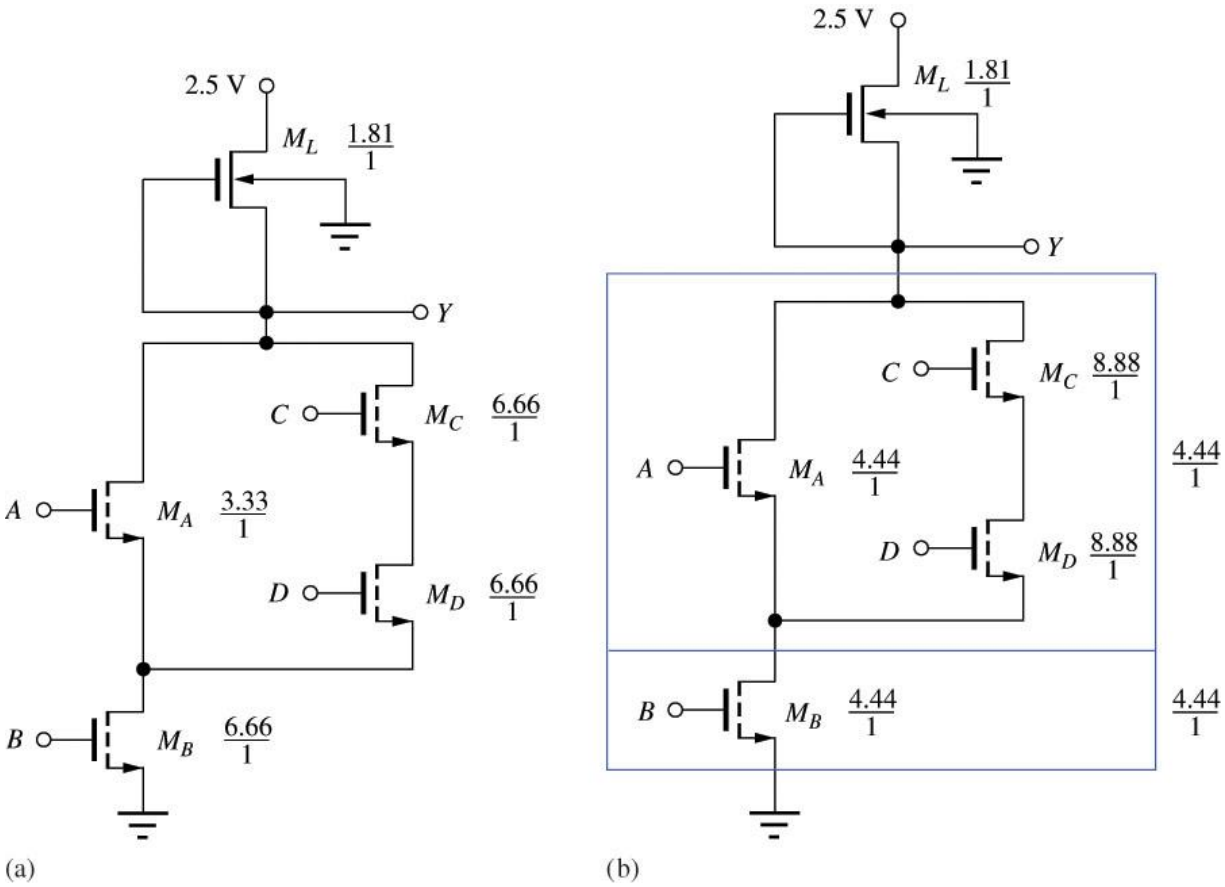
Sadly, most modern IC foundries are now forbidding designers to express themselves in this way over concerns about design rule violations and potential processing problems. Designers tell us that this has forced them to become covert with their doodles and they are sometimes embedding the graphics directly into functional design structures.

Complex Logic Gate Transistor Sizing

- There are two ways to find the W/L ratios of the switching transistors

1) Use the worst-case path (most devices in series) and choose the W/L ratios to achieve the value of R_{on} equivalent to that of the inverter
2) Partitioning the circuit into a series sub-networks, and make the equivalent on-resistances equal

Complex Logic Gate Transistor Sizing



The figure on the left shows the worst case technique to find the sizes where $(W/L)_S = 2.06$ is the reference inverter ratio for this technology and the longest path is 3 transistors are in series

The figure on the right shows the partitioning technique to find the sizes which gives two 4.12/1 ratios in series which is 2(2.06/1)

Static Power Dissipation

- Static Power Dissipation is the average power dissipation of the logic gate for the high and low logic states:

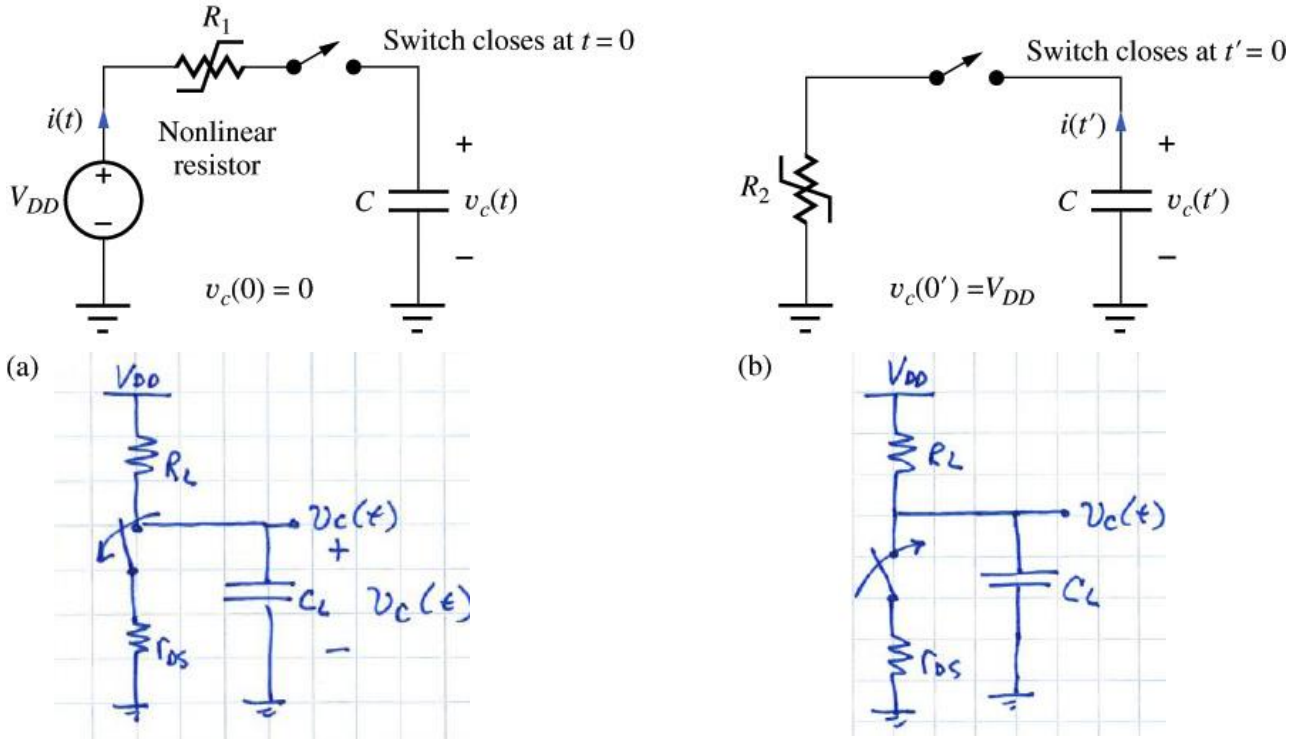
$$P_{av} = \frac{V_{DD} I_{DDH} + V_{DD} I_{DDL}}{2}$$

- I_{DDH} = current in the circuit for $v_O = V_H$
- I_{DDL} = current in the circuit for $v_O = V_L$

- Since $I_{DDH} = 0$ A for $v_O = V_H$: $P_{av} = \frac{V_{DD} I_{DDL}}{2}$

Dynamic Power Dissipation

- Dynamic Power Dissipation is the power dissipated during the process of charging and discharging the load capacitance connected to the logic gate



Charging

Discharging

Dynamic Power Dissipation

- Based on the energy equation, the energy delivered to the capacitor can be found by:

$$E_D = V_{DD}\int_0^{\infty} i(t)dt = CV_{DD}\int_{V_C(0)}^{V_C(\infty)} dv_C = CV_{DD}^2$$

- The energy stored by the capacitor is:

$$E_S = \frac{CV_{DD}^2}{2}$$

- The energy lost in the resistive elements is given by:

$$E_L = E_D - E_S = \frac{CV_{DD}^2}{2}$$

Dynamic Power Dissipation

- The total energy lost in the first charging and discharging of the capacitor through resistive elements is given by:

$$E_{TD} = \frac{CV_{DD}^2}{2} + \frac{CV_{DD}^2}{2} = CV_{DD}^2$$

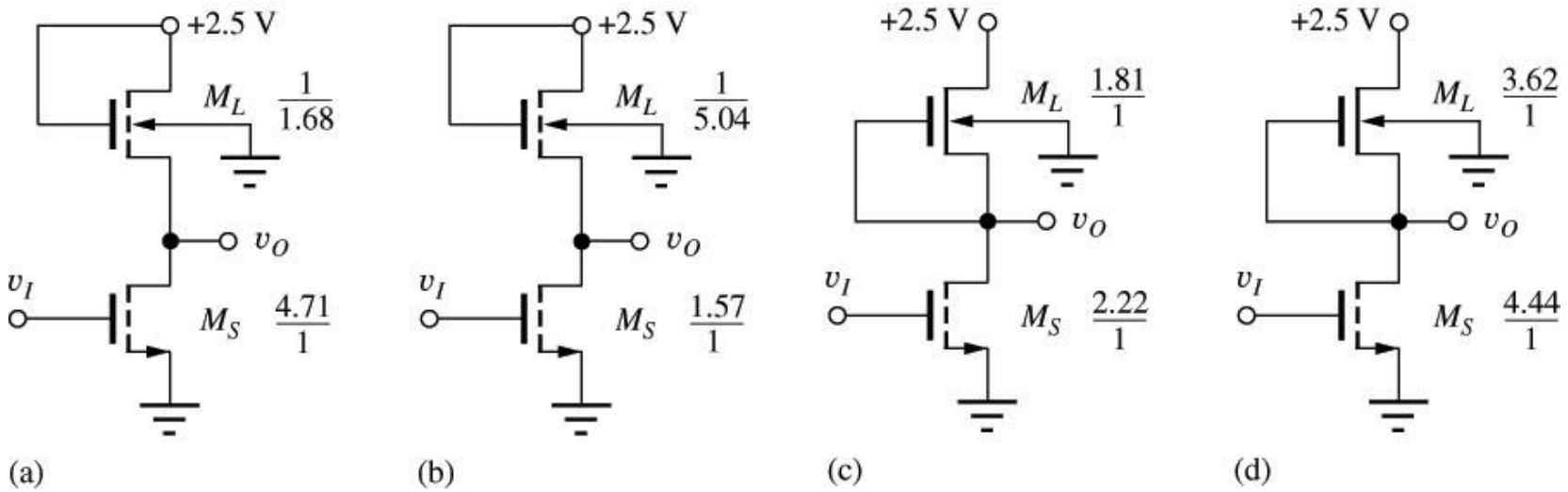
- Thus, if the logic circuit is switching at a frequency *f*, the dynamic power dissipation is given by:

$$P_D = CV_{DD}^2 f$$

Power Scaling in MOS Logic

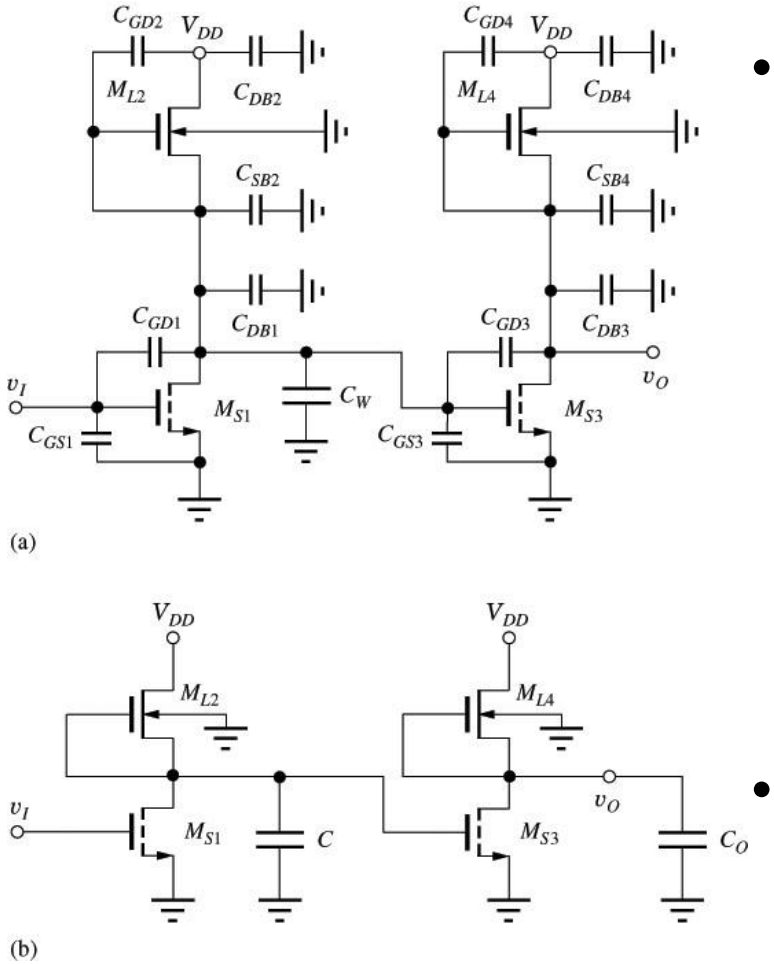
- By reducing the W/L of the load **and** switching transistors of an inverter, it is possible to reduce the power dissipation by the same factor without sacrificing V_H and V_L.
- This same concept works for increasing the power which will increase the dynamic response.

Power Scaling in MOS Logic



a) Original Saturated Load Inverter
b) Saturated Load inverter designed to operate at 1/3 the power
c) Original Depletion-Mode Inverter
d) Depletion-mode inverter designed to operate at twice the power

Dynamic Behavior
Capacitance in MOS Logic Circuits



- The MOS device has capacitances C_{SB}, C_{GS}, C_{DB}, and C_{GD} that need to be considered for dynamic response analysis, but depending on the configuration, some of them will be shorted.
- The capacitances seen at a node can be lumped together.

Fan-out Limitations

- DC loading constraints are not usually important for MOS logic circuits since they normally drive capacitive loads (i.e. the gate of a MOS)
- As the number of gates the output (fan-out) of a logic device has to drive, the load capacitance increases, and the time response degrades
- This notion implies that the fan-out that a logic circuit can drive will be limited to time delay tolerances of the circuit

Υπολογισμός delay στη φόρτιση/ εκφόρτιση πυκνωτή

- Ποιά είναι η αλλαγή του φορτίου πυκνωτή C κατά την φόρτιση/ εκφόρτιση του όπου αλλάζει η τάση κατά ΔV ?

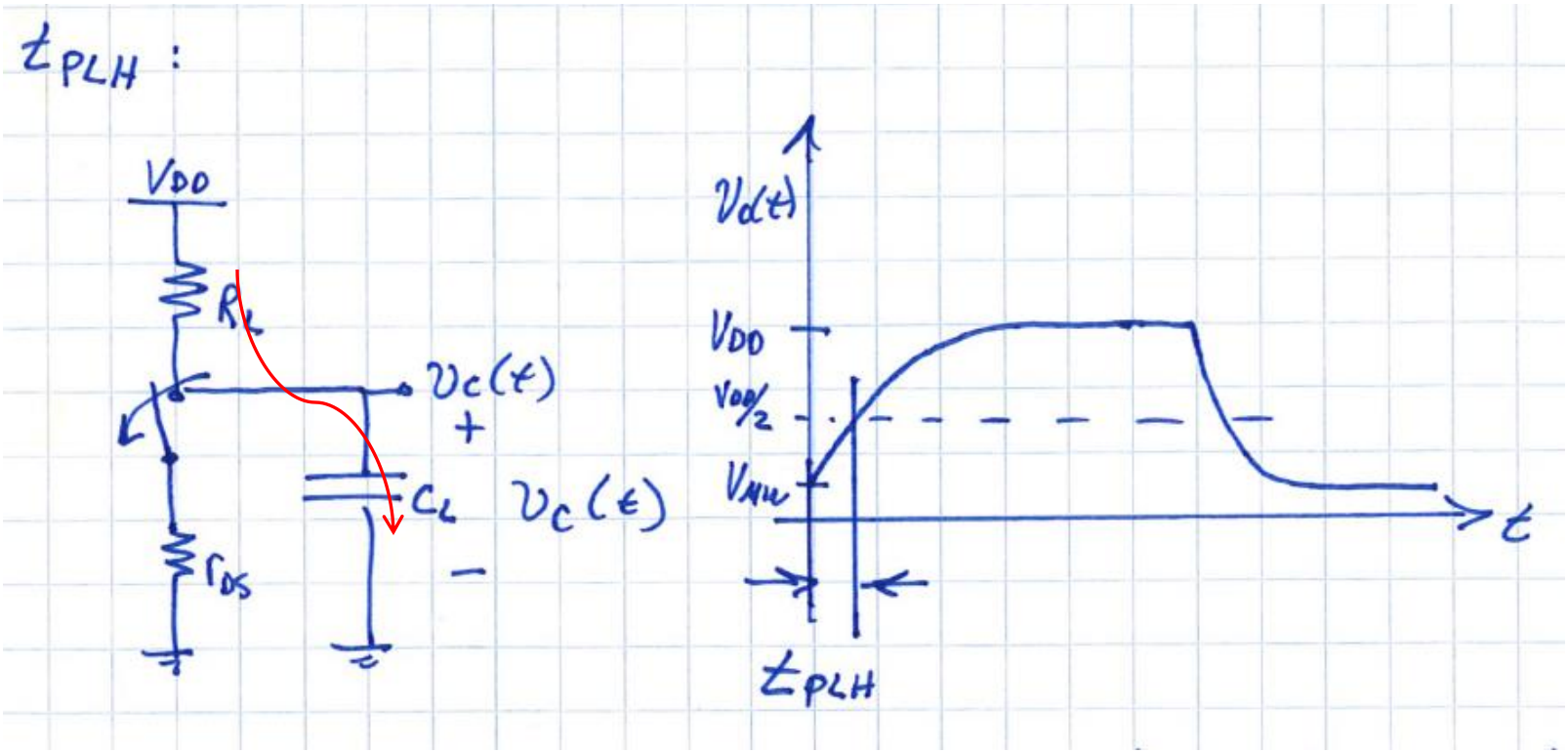
$$\Delta Q = C*(\Delta V)$$

Επειδή $dQ(t)/dt = I(t)$

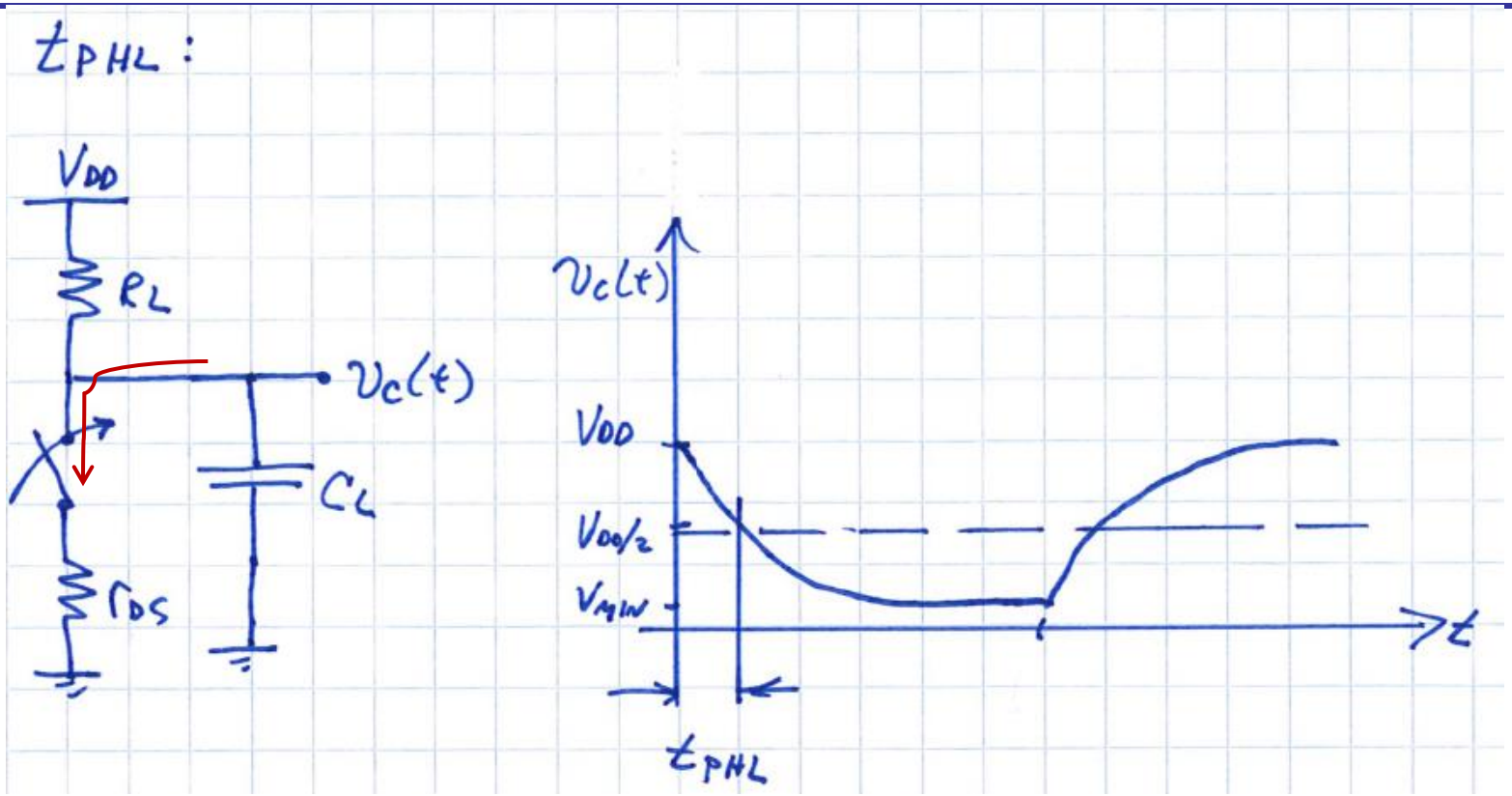
τότε ο χρόνος Δt που απαιτείται για την αλλαγή του φορτίου (και κατά συνέπεια και της τάσης) είναι κατά προσέγγιση

$\Delta Q(t)/\Delta t$ = μέσο ρεύμα = I_m

Dynamic Response of the NMOS Inverter with a Resistive Load (I)



Dynamic Response of the NMOS Inverter with a Resistive Load (II)



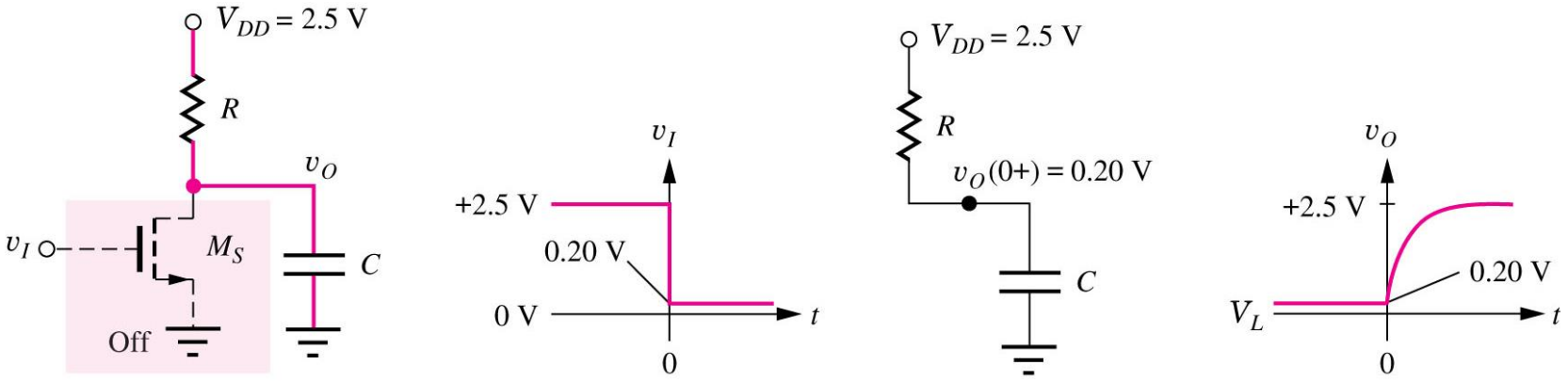
Dynamic Response of the NMOS Inverter with a Resistive Load (III)

- Rise time is defined as the time for the output to change from 10% to 90% of the complete transition.

$$V_I + 0.1\Delta V = V_F - \Delta V \exp\left(\frac{-t_1}{RC}\right) \quad yields \quad t_1 = -RC\ln 0.9$$

$$V_I + 0.9\Delta V = V_F - \Delta V \exp\left(\frac{-t_2}{RC}\right) \quad yields \quad t_2 = -RC\ln 0.1$$

$$t_r = t_2 - t_1 = RC\ln 9 = 2.2RC$$



Dynamic Response of the NMOS Inverter with a Resistive Load (I)

- Delay time is defined as the time required for the output to change 50%. Using a similar analysis we get the following results for rise/fall times and propagation delay:

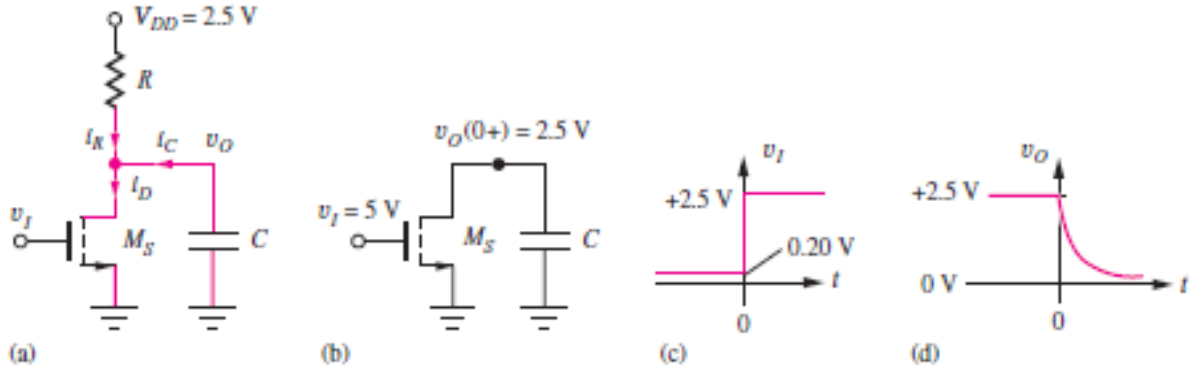
$$t_r = t_f = 2.2RC \qquad \tau_{PLH} = \tau_{PHL} = 0.69RC$$

where R and C are the resistance and capacitance seen at the output. For low-to-high transitions, R is the load resistance (M_S is off). For high-to-low transitions, the on resistance of M_S, R_{onS}, varies during the transition but an effective R, R_{eff}, can be approximated as 1.7 R_{onS} from SPICE simulation.

$$\tau_{PHL} = 0.69R_{\text{eff}}C \approx 1.2R_{onS}C \qquad t_f = 2.2R_{\text{eff}}C \approx 3.7R_{onS}C,$$

$$where\ R_{\text{eff}} = 1.7R_{onS}$$

Dynamic Response of the NMOS Inverter with a Resistive Load (II)



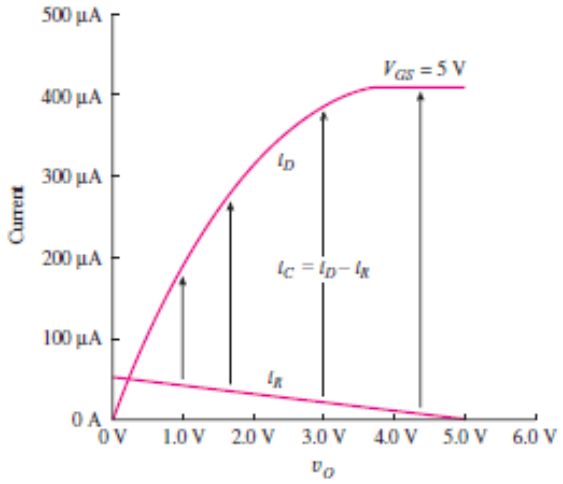


Figure 6.42 Drain current and resistor current versus v_O.

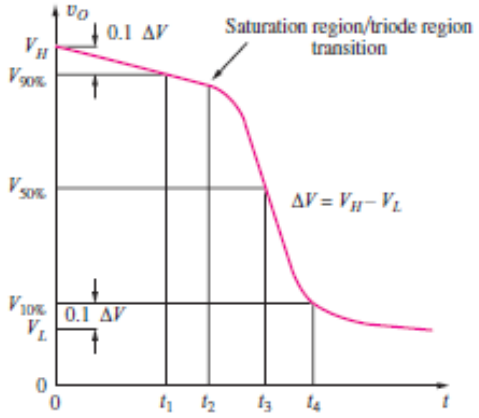
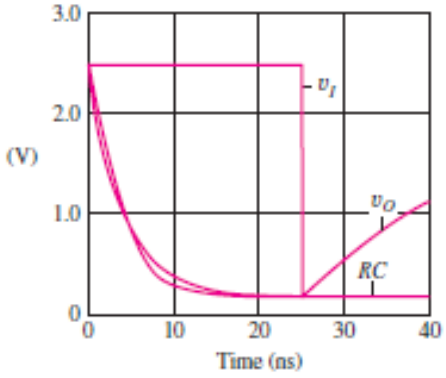


Figure 6.43 Times needed for calculation of τ_{PHL} and t_f for the inverter. Fall time $t_f = t_4 - t_1$; propagation delay $\tau_{PHL} = t_3$.

$i_C = i_D - i_R$

Το ρεύμα i_D του υποδοχέα πολύ μεγαλύτερο του ρεύματος i_R στην αντίσταση

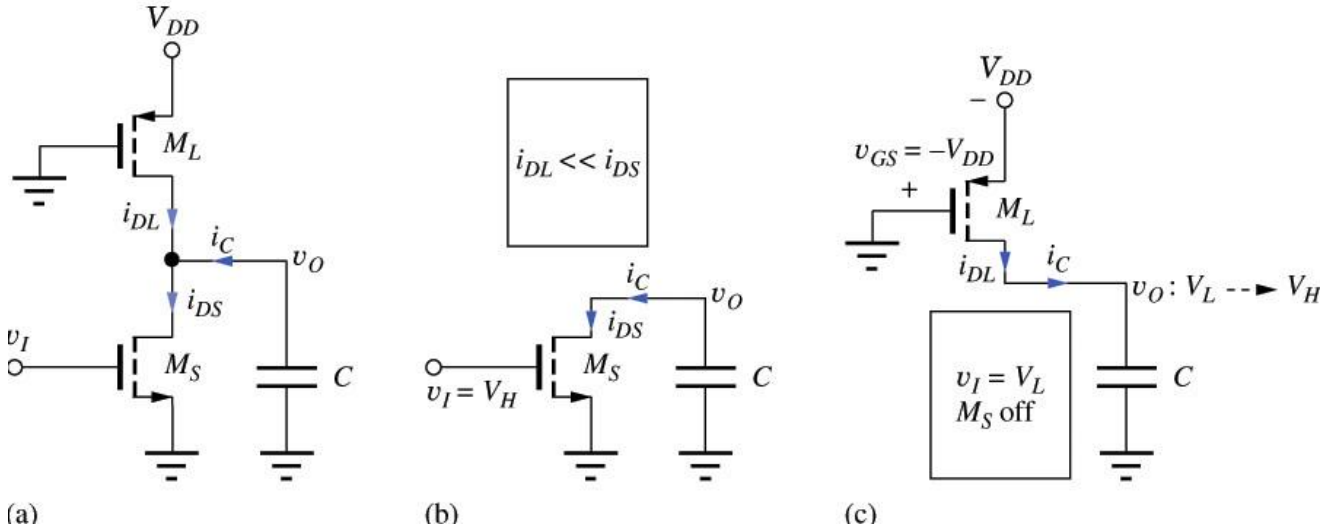
Dynamic Response of the NMOS Inverter with a Resistive Load (III)



Προσομοίωση SPICE για high-to-low transition για αναστροφέα με φορτίο αντίσταση με τιμή R = 28.8kΩ και $(W/L)_S = 2.22/1$. Η δεύτερη καμπύλη δείχνει τη μεταβατική απόκριση εκθετικής εκφόρτισης κυκλώματος RC με τιμή $R = R_{eff}$

$$R = R_{eff} = 1.7R_{onS}, \quad R_{onS} = 1/K_n(V_H - V_{TNS})$$

Pseudo NMOS Inverter - Dynamic Response



$$\tau_{PHL} = 0.69 R_{\text{eff}} C \approx 1.2 R_{onS} C \qquad \tau_{PLH} = 0.69 R_{\text{eff}} C \approx 1.2 R_{onL} C$$

$$t_f = 2.2 R_{\text{eff}} C \approx 3.7 R_{onS} C, \qquad t_r = 2.2 R_{\text{eff}} C \approx 3.7 R_{onL} C,$$

Voltage Transfer Characteristic

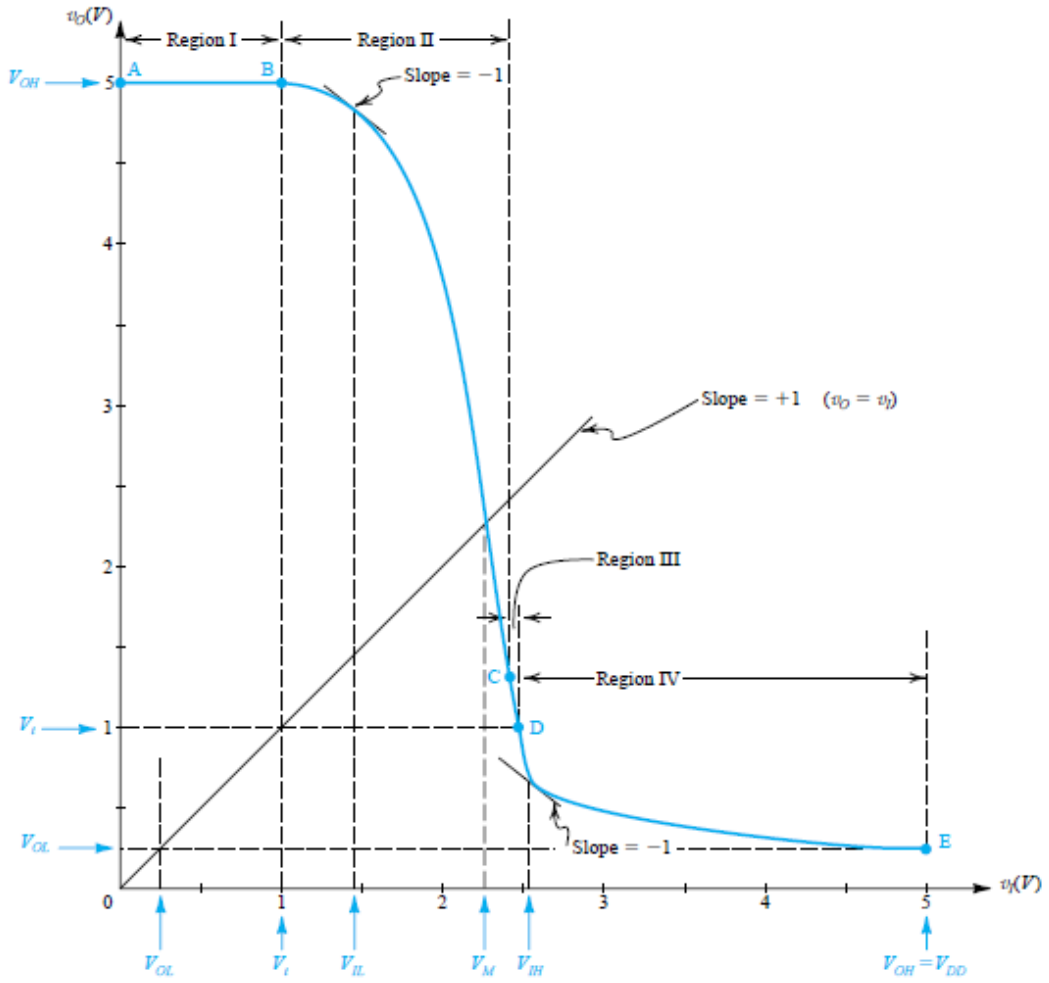


Figure 14.3 VTC for the pseudo-NMOS inverter. This curve is plotted for $V_{DD} = 5$ V, $V_{tn} = -V_{tp} = 1$ V, and $r = 9$.

Pseudo NMOS Inverter - Dynamic Response Example

- Find t_f, t_r, τ_{PHL}, τ_{PLH} for a pseudo NMOS inverter where:
  - $(W/L)_S = 2.22/1$ and $(W/L)_L = 1.11/1$
  - $C_{LOAD} = 1$ pF
  - $V_{TN} = 0.6$ V and $V_{TP} = -0.6$ V
  - $V_{DD} = 2.5$ V
  - $K_n = (2.06)(100 * 10^{-6}\ A/V^2)$
  - $K_L = (1.11)(40 * 10^{-6}\ A/V^2)$

Pseudo NMOS Inverter - Dynamic Response Example

- First find the on-resistances of the two switch and load devices

$$R_{onS} = \frac{1}{K_S(V_H - V_{TNS})} = \frac{1}{(2.22)\left(100\frac{\mu A}{V^2}\right)(2.5-0.6)} = 2.37k\Omega$$

$$R_{onL} = \frac{1}{K_L(|-VDD - VTP|)} = \frac{1}{(1.11)\left(40\frac{\mu A}{V^2}\right)(|-2.5-(-0.6)|)} = 11.9k\Omega$$

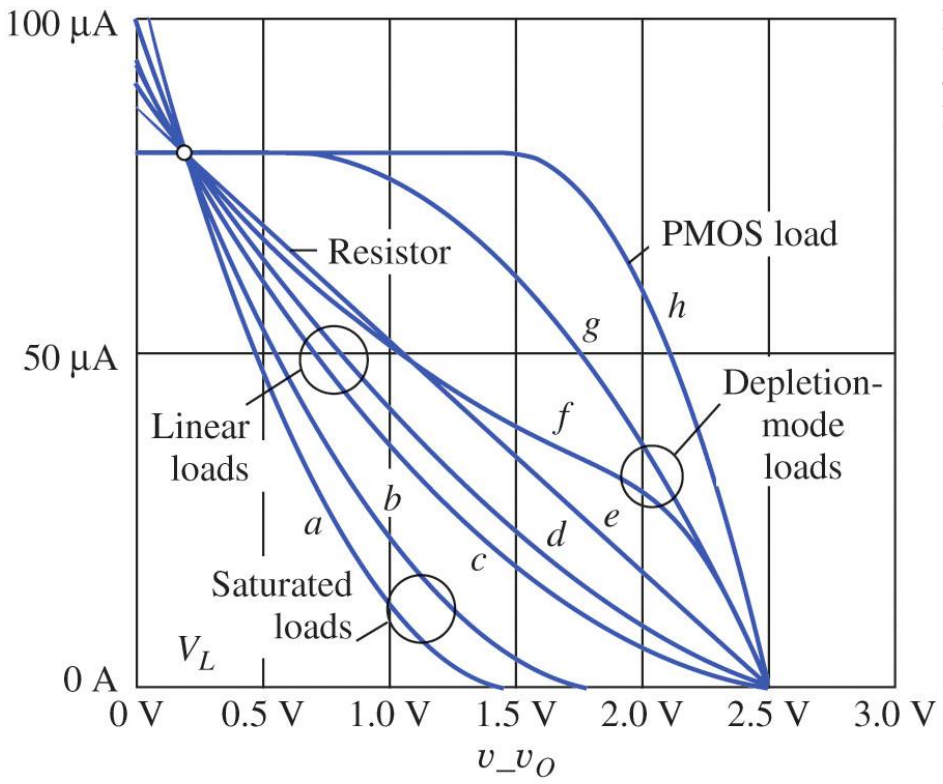
NMOS Inverter with a Depletion-Mode Load - Dynamic Response Example

- Now calculate delays from the R_{eff} approximations:

$$\tau_{PHL} = 1.2R_{onS}C = 1.2(2.37K)(1pF) = 2.84 \ \ ns$$
$$\tau_f = 3.7R_{onS}C = 8.77 \ \ ns$$
$$\tau_{PLH} = 1.2R_{onL}C = 1.2(11.9K)(1pF) = 14.3 \ \ ns$$
$$\tau_r = 3.7R_{onL}C = 44.0 \ \ ns$$

SPICE simulations show good agreement and result in values of 3 ns, 7 ns, 15.0 ns, and 35.0 ns.

Comparison of Load Devices



NMOS Inverter Time Delays

	τ_{PHL}	τ_{PLH}	t_f	t_r
Resistor load	$1.2R_{onS}C$	$0.69RC$	$3.7R_{onS}C$	$2.2RC$
Pseudo NMOS	$1.2R_{onS}C$	$1.2R_{onL}C$	$3.7R_{onS}C$	$3.7R_{onL}C$
Depletion load	$1.2R_{onS}C$	$3.6R_{onL}C$	$3.7R_{onS}C$	$8.1R_{onL}C$
Saturated load	$1.2R_{onS}C$	$3.0R_{onL}C$	$3.7R_{onS}C$	$11.9R_{onL}C$
Linear load	$1.2R_{onS}C$	$0.69R_{onL}C$	$3.7R_{onS}C$	$3.7R_{onL}C$

$$R_{onS} = \frac{1}{K_S(V_H - V_{TNS})} \qquad R_{onL} = \frac{1}{K_L|V_{GS} - V_{TNL}|}$$

The current has been normalized to 80 μA for

$v_o = V_{OL} = 0.20$ V

in the figure for the various types of inverters

Comparison of Load Devices

- The saturated load devices have the poorest fall time since they have the lowest load current delivery
- The saturated load devices also reach zero current before the output reaches 2.5 V
- The linear load device is faster than the saturated load device, but about equal to the resistive load speed.
- The fastest τ_{PLH} is for the pseudo NMOS device as a result of the PMOS device

Gate Device Geometry Scaling based Upon Reference Circuit Simulation

- State-of-the-art short gate length technologies are hard to analyze
- Scaling can be used to properly set W/L for a given load capacitance relative to reference gate simulation with a reference load.

$$\tau_P = \frac{(W/L)}{(W/L)'} \times \left(\frac{C_L'}{C_{Lref}}\right) \times \tau_{\Pr ef} \quad or \quad \left(\frac{W}{L}\right)' = \left(\frac{W}{L}\right) \times \left(\frac{\tau_{\Pr ef}}{\tau_P}\right) \times \left(\frac{C_L'}{C_{Lref}}\right)$$

Scaling allows us to calculate a new geometry (W/L)' in terms of a target load and delay.

Pseudo NMOS Propagation Delay - Design Example

- Design a pseudo NMOS inverter with a propagation delay (τ_P) of 2 ns when driving a capacitance of 5 pF, and find $(W/L)_S$, $(W/L)_L$, t_f, and t_r for:
  - $C_{LOAD} = 5$ pF
  - $V_{TN} = 0.6$ V and $V_{TP} = -0.6$ V
  - $V_{DD} = 2.5$ V, $V_H = 2.5$ V and $V_L = 0.20$ V
  - Base on a reference inverter with:
    - $(W/L)_S = 2.22/1$
    - $(W/L)_L = 1.11/1$
  - Use equations from Table 6.10

Propagation Delay - Design Example

$$\tau_p = \frac{1.2R_{onS}C + 1.2R_{onL}C}{2} = \frac{0.6C}{2K_n}\left[\frac{1}{(V_{DD} - V_{TN})} + \frac{1}{\frac{K_p}{K_n}(|-V_{DD} - V_{TP}|)}\right]$$

$$\left(\frac{W}{L}\right)_S = \frac{0.6(5pF)}{2ns(100uA/V^2)}\left[\frac{1}{(2.5-0.6)} + \frac{1}{\frac{1.11(40)}{2.22(100)}(|-2.5-(-0.6)|)}\right] = \frac{47.4}{1}$$

$$\left(\frac{W}{L}\right)_L = \frac{1}{2}\left(\frac{W}{L}\right)_S = \frac{23.7}{1}$$

$$\tau_f = 3.7R_{onS}C = 3.7\frac{5pF}{47.4(100\mu A/V_2)(2.5-0.6)V} = 2.05 \ \ ns$$

$$\tau_r = 3.7R_{onL}C = 3.7\frac{5pF}{23.7(40\mu A/V_2)(|-2.5-(-0.6)|)V} = 10.3 \ \ ns$$