

**Projects about Quantum adder circuits  
Final examination – June 2018**

*Quirk Simulator*

<http://algassert.com/2016/05/22/quirk.html>

**PROBLEM TO SOLVE**

1. The HNG gate is described in reference: *Haghparast M. and K. Navi, 2008. A Novel reversible BCD adder for nanotechnology based systems. Am. J. Applied Sci., 5 (3): 282-288.*  
<http://thescipub.com/pdf/10.3844/ajassp.2008.282.288>
2. The operation of the HNG gate is shown in Figure 1, where each output is annotated with the corresponding logic expression. Observe that two input variables are also outputs. HNG gate can be used for implementing all Boolean functions.

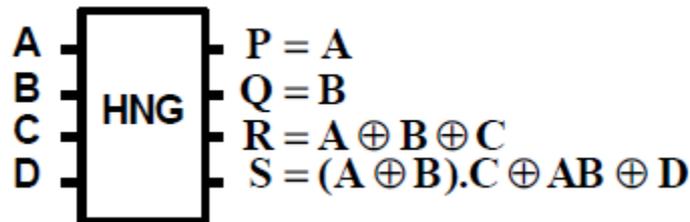


Fig. 1. Quantum circuit model of the HNG gate.

The corresponding truth table of the HNG gate is depicted in Table 1.

Table 1. The truth table of HNG gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	1	0	0	1
1	0	1	1	1	0	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	0	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	0

A total of four reversible gates are required to build the quantum circuit of the HNG gate, as depicted in Fig.2:

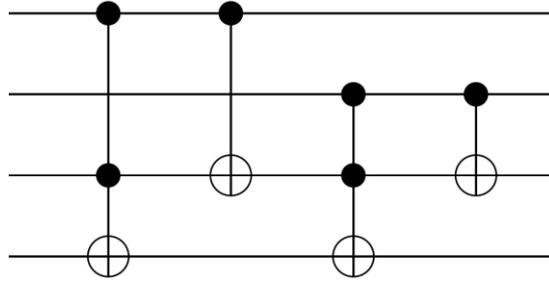


Fig. 2. Quantum circuit model of the HNG gate.

The OR and the X-NOR functions can be simultaneously implemented on HNG (Fig. 3).

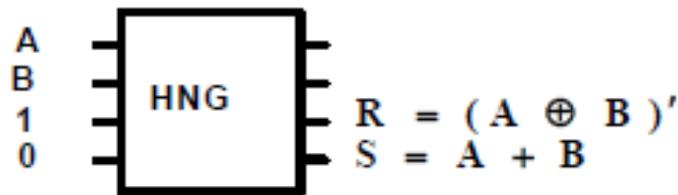


Fig.3 XNOR and OR.

The XOR function and the NAND function can be implemented as depicted in Fig.4.

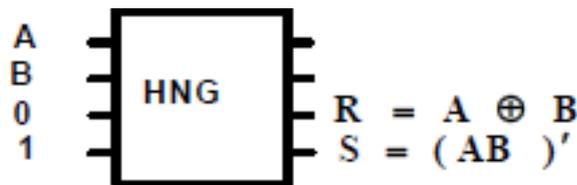


Fig.4 XOR and NAND gates.

The NOR function can be obtained as shown in Fig. 5.

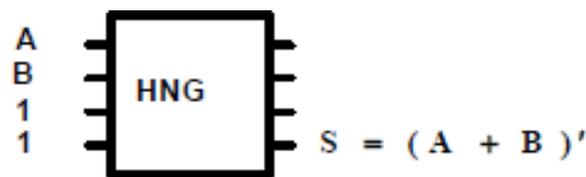


Fig.5 XOR gate.

The implementation of the HNG gate as NOT function is shown in Fig.6.

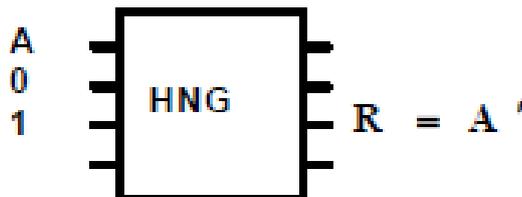


Fig.6 NOT gate.

The AND function can be implemented as depicted in Fig.7.

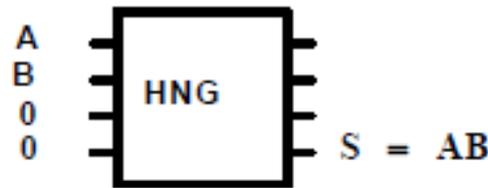


Fig.7 AND gate.

Full adder circuit is a versatile and widely used element in digital arithmetic processing. One of the prominent functionalities of the HNG gate is that it can work singly as a reversible full adder unit. The implementation of HNG gate as the reversible full adder is depicted in Fig.8.

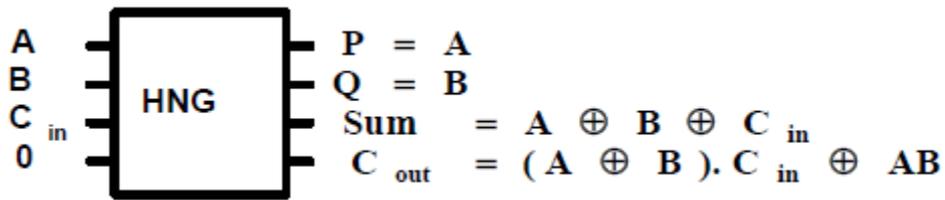


Fig.8 The HNG gate is a 4-bit reversible gate, which is a full adder.

In Quirk simulation, create a circuit with the minimum cost (number of gates from Clifford-T library), including Bloch spheres as well. Use *all the possible eight input states* to prove that works as a full adder. Save your circuit simulation in a video mp4 file that implements all eight input states, and write a report. Draw a circuit indicating the implementation of each CCNOT and CNOT gate in Fig.2 by placing in boxes the equivalent combination of Quirk gates. Explain the operations of your circuit in each case. Include the corresponding truth tables.

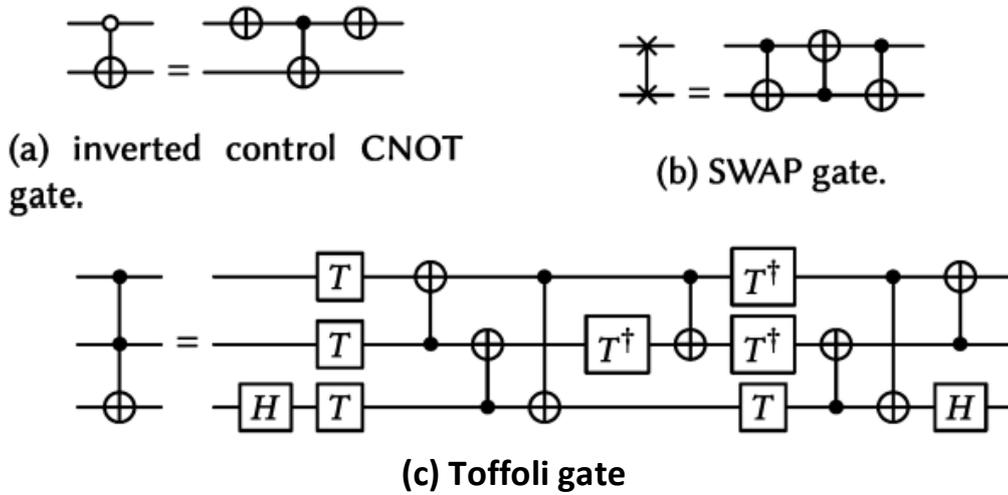
### Supplementary Information

The fault tolerant Clifford+T gate set is used in fault tolerant quantum circuit design. Table 1 shows the gates that make up the Clifford+T gate set.

Table 1. The Clifford + T gates

Type of Gate	Symbol	Matrix
NOT gate	$N$	$\begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$
Hadamard gate	$H$	$\frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$
$T$ gate	$T$	$\begin{bmatrix} 1 & 0 \\ 0 & e^{i \cdot \frac{\pi}{4}} \end{bmatrix}$
$T$ gate Hermitian transpose	$T^\dagger$	$\begin{bmatrix} 1 & 0 \\ 0 & e^{-i \cdot \frac{\pi}{4}} \end{bmatrix}$
Phase gate	$S$	$\begin{bmatrix} 1 & 0 \\ 0 & i \end{bmatrix}$
Phase gate Hermitian transpose	$S^\dagger$	$\begin{bmatrix} 1 & 0 \\ 0 & -i \end{bmatrix}$
CNOT gate	$C$	$\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix}$

The Clifford+T implementation of the inverted control CNOT gate, SWAP gate and Toffoli gate are shown in figure A.

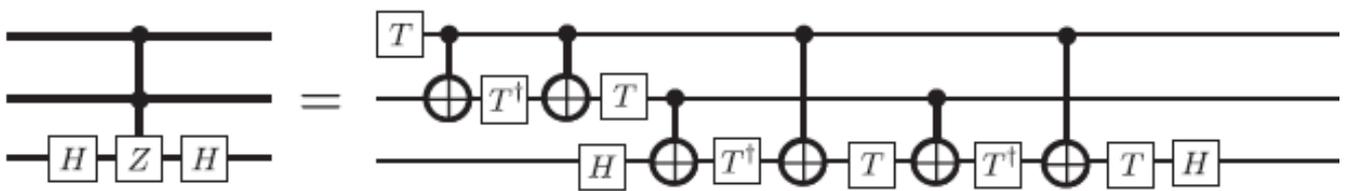


**Fig.A** The fault tolerant Clifford + T implementations of quantum logic gates.

Fault tolerant quantum circuit performance is evaluated in terms of T-count because the implementation costs of the T gate is significantly greater than the implementation costs of the other Clifford+T gates.

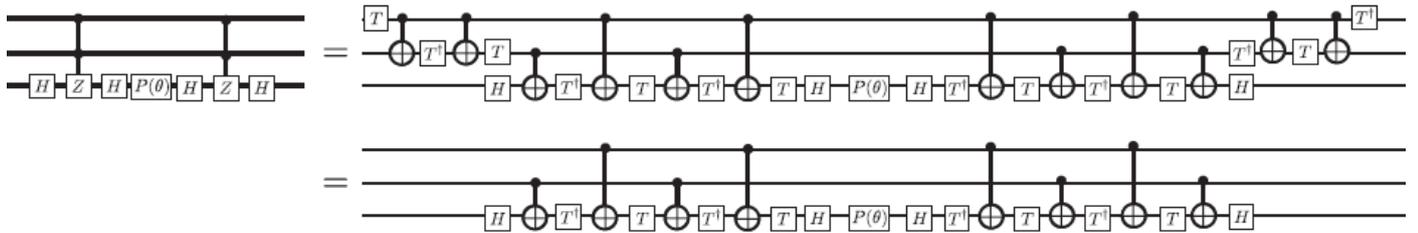
T-count is the total number of T gates or Hermitian transposes of the T gate in a quantum circuit. As illustrated in figure A, the inverted control CNOT gate and the SWAP gate both have a T-count of 0 while the Toffoli gate has a T-count of 7.

Figure B shows the **exact** Clifford+T decomposition of the Toffoli gate using 7 T gates. Note that we have used the identity  $HZH=X$  to rewrite the Toffoli as a double-controlled-Z gate, which is diagonal and hence has an exact decomposition in the Clifford+T basis.



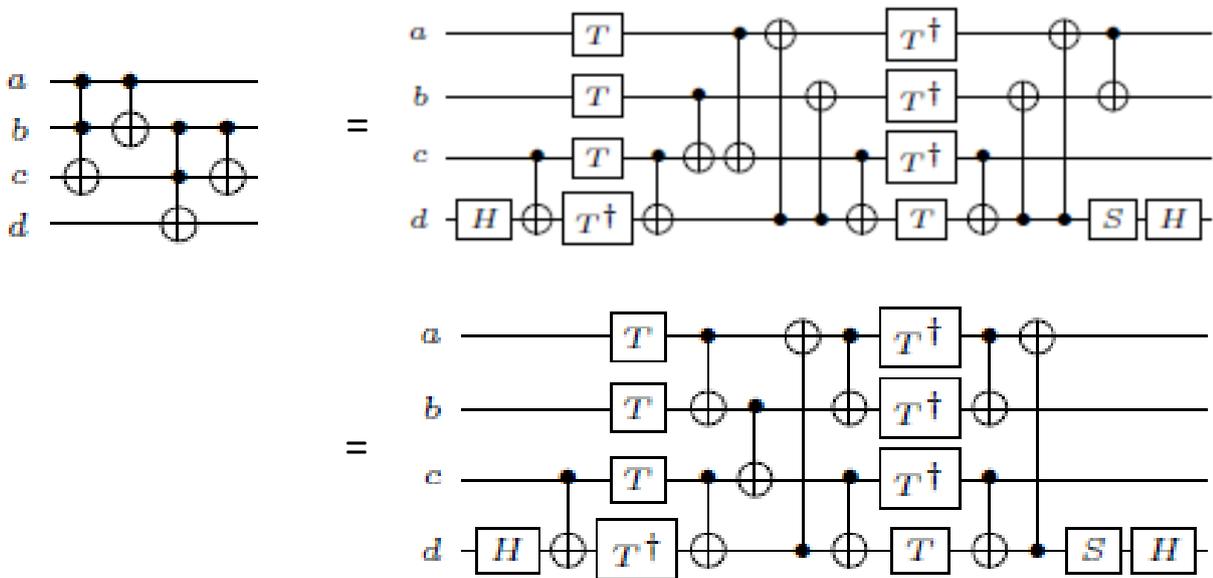
**Fig.B** An exact decomposition of the Toffoli gate on the Clifford+T basis. We use the fact that  $HZH=X$ , where H is the Hadamard gate and Z, X are the standard Pauli gates.

Figure C shows an exact decomposition of two paired Toffoli gates with a phase gate on the target qubit. We use the Clifford+T decomposition of the Toffoli shown in Figure B. The first two qubits in this example have a sequence of gates which are adjoints of one another, thus if we carry through all commutations to move the gates on the top two qubits towards the center, we find that not only do they mutually cancel one another, but all commutations in between different CNOT operators will also mutually cancel. Independently they would cost 7 T gates each for a total of 14 per pair, however *in this paired configuration a pair of matched Toffoli entanglers costs only 8 T gates.*



**Fig.C** An exact decomposition of two paired Toffoli gates with a phase gate on the target qubit.

As another example consider the reversible full adder circuit below, where each Toffoli-CNOT pair is in fact a Peres gate:

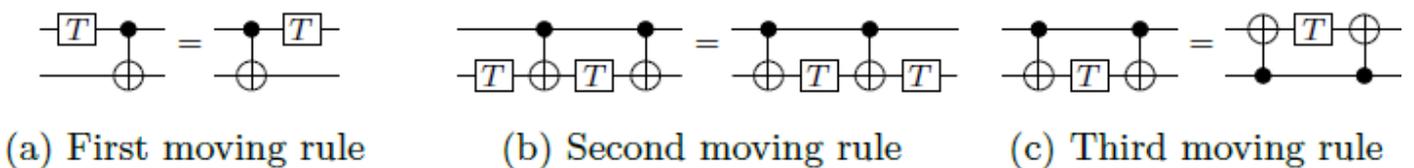


**T gate parallelization** means moving T and  $T^\dagger$  gates, each on a unique circuit line, to the same circuit level so that they can operate in parallel.

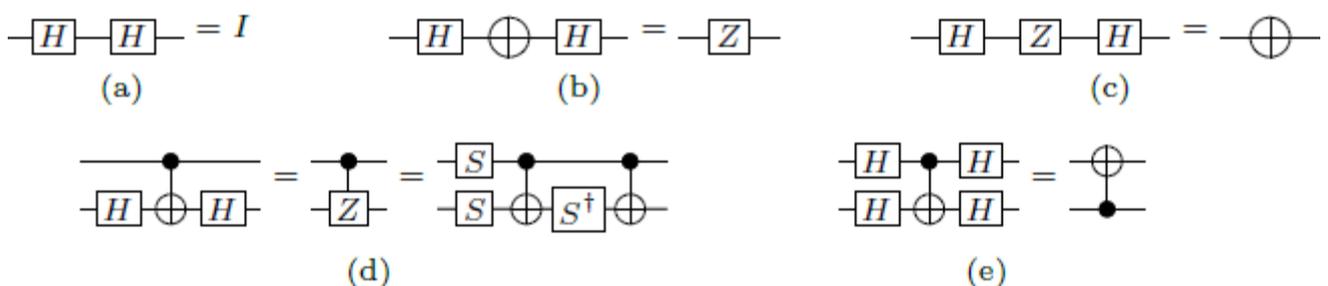
### Appendix A

Optimizations in the Clifford+T library.

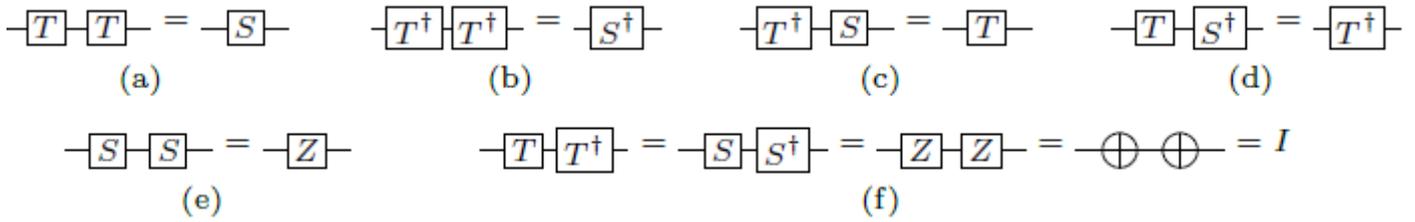
#### B.1 Moving rules for the Clifford+T gates



#### B.2 Reduction rules for the H gates



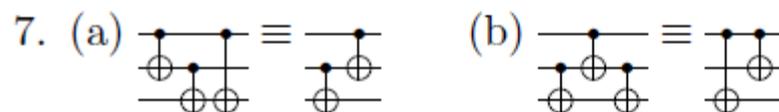
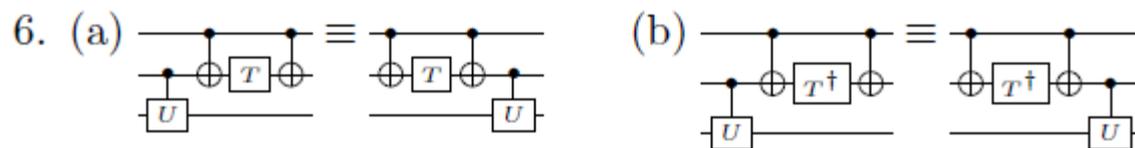
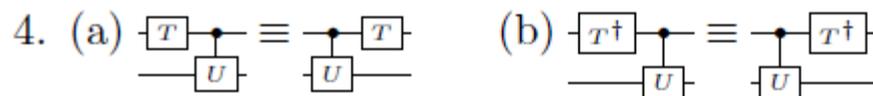
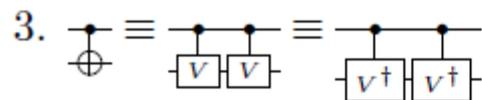
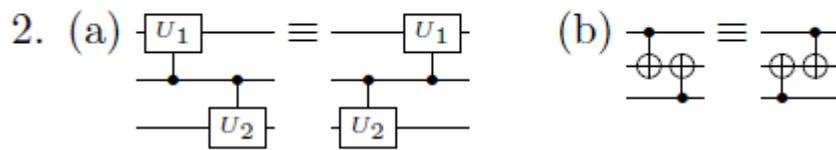
### B.3 Reduction rules for the remaining gates



### Appendix B

Quantum gate properties:

1. (a)  $H = H^{-1}$       (b)  $S = TT$       (c)  $S^\dagger = T^\dagger T^\dagger$



**Property 5:** Note that the three gates in the structure have a common target and the two CNOTs have a common control.

**Property 6** provides considerable flexibility in moving gates. It is a direct consequence of Properties 4 and 5.

**Property 7** gives two important identities for reducing the number of CNOT gates in a circuit.

**Property 7(a)** describes the interchanging of 2 CNOTs which share a qubit as target for one and control for the other. This introduces a third CNOT with control and target from the unshared lines of the initial pair of gates.